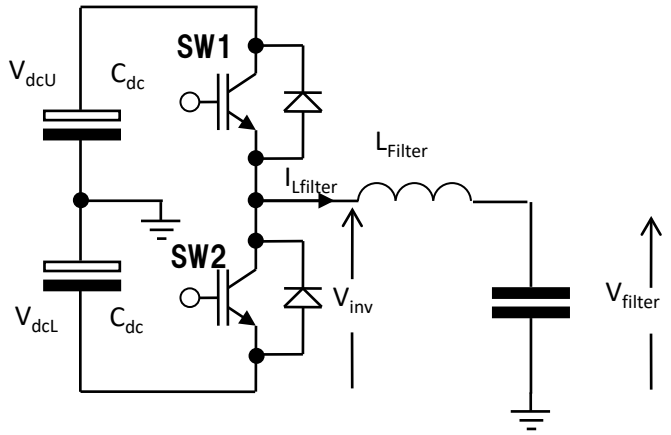
Digital Electric Engineering for Digital Grid

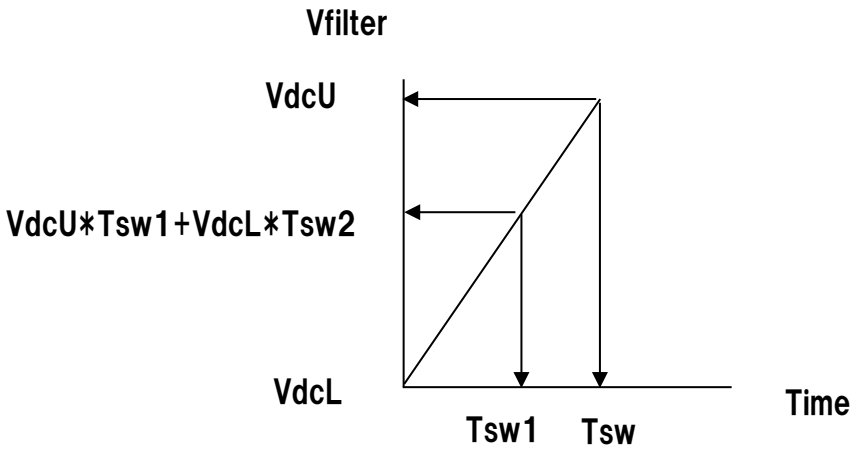
May 30, 2024
At University of Moratuwa

Dr. Rikiya ABE
CEO, DG Capital Group Inc.
Representative Director, Digital Grid Consortium

目次

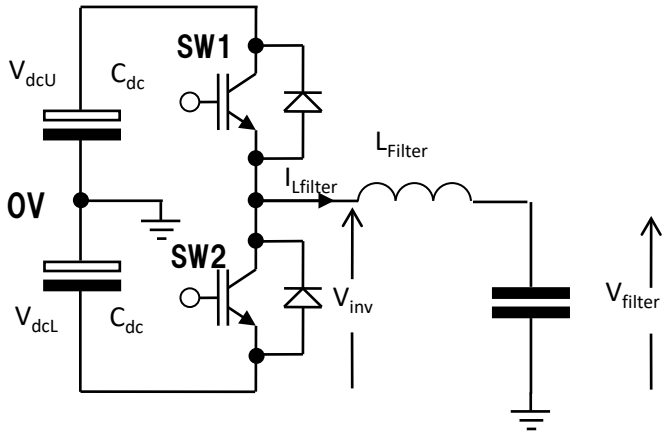
(1) Half Bridge Inverter



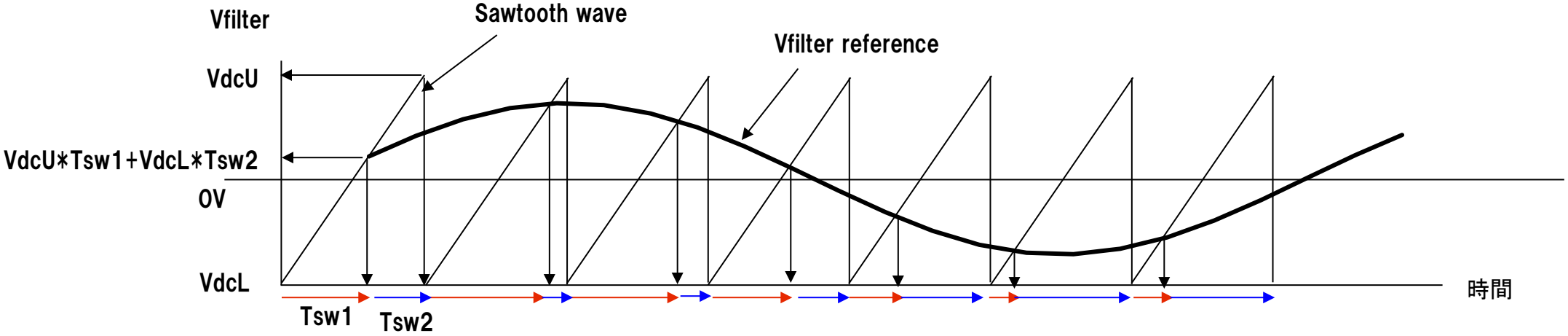


- **Half Bridge Inverter**
  - SW1:ON & SW2:OFF -> Vinv=VdcU
  - SW1:OFF & SW2:ON -> Vinv=VdcL
  - Vfilter=> average of Vinv
  - Averaged by Lfilter and Cfilter
- **SW on Duty**
  - Switching frequency: fsw
  - Duty Cycle: Tsw=1/fsw
  - On duty of SW1=Tsw1
  - On duty of SW2=Tsw-Tsw1=Tsw2
  - Vfilter=VdcU*Tsw1+VdcL*Tsw2
- **Example: VdcU=50V, VdcL=-50V (VdcL<=0)**
  - When Tsw1=1/2*Tsw=Tsw2, Vfilter=0V
  - When Tsw1=Tsw, Tsw2=0, Vfliter=50V
  - When Tsw1=3/4*Tsw, Tsw2=1/4*Tsw, Vfliter=25V
- **Duty target for the target Voltage**
  - Vfilter=VdcU*Tsw1+VdcL*(Tsw-Tsw1)
  - Tsw1/Tsw=D1, then
  - Vfilter/Tsw=VdcU*D1+VdcL*(1-D1)
  - =(VdcU-VdcL)*D1+VdcL

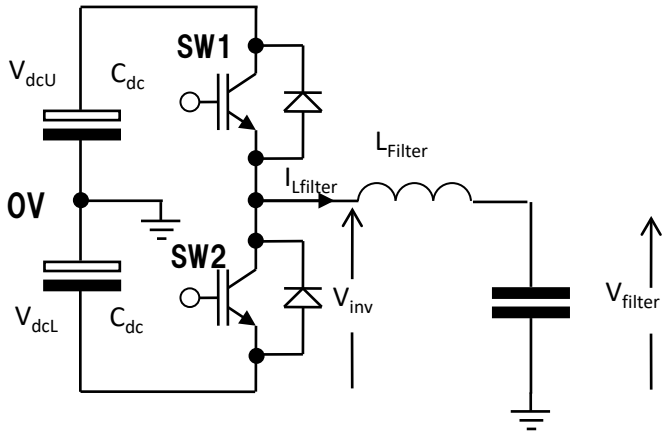
(2) PWM control of Voltage



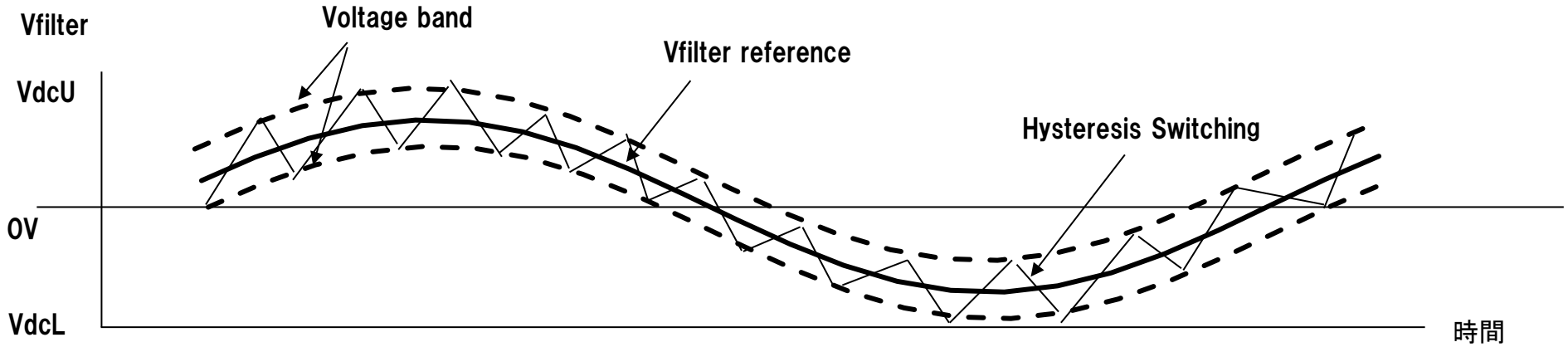
- **PWM: Pulse Width Modulation**
  - Set the Vfilter reference -> calculate Duty cycle
  - Sawtooth wave is used for determine Tsw1 in comparison with Vfilter reference
- **PWM control of Voltage**
  - Analog comparator is useful for PWM switching
  - Comparator compares Vfilter reference and sawtooth wave



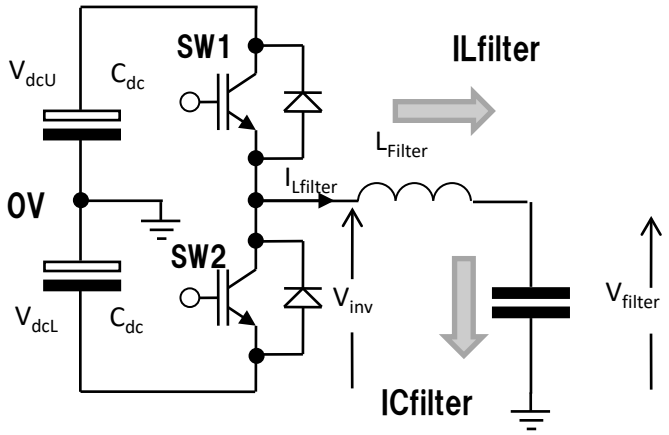
(3) Hysteresis control of Voltage



- **Hysteresis Switching**
  - Set Vfilter reference
  - Set Voltage band
- **Hysteresis mechanism**
  - Sw1 ON until Vfilter measured exceeds upper voltage band
  - Sw1 OFF and Sw2 ON until Vfilter measured exceeds lower voltage band
  - Sw1 ON and Sw2 OFF and repeat
- **Disadvantage**
  - Voltage measurement with narrow band won't be accurate



(4) Hysteresis control of Current



Hysteresis Switching of Current

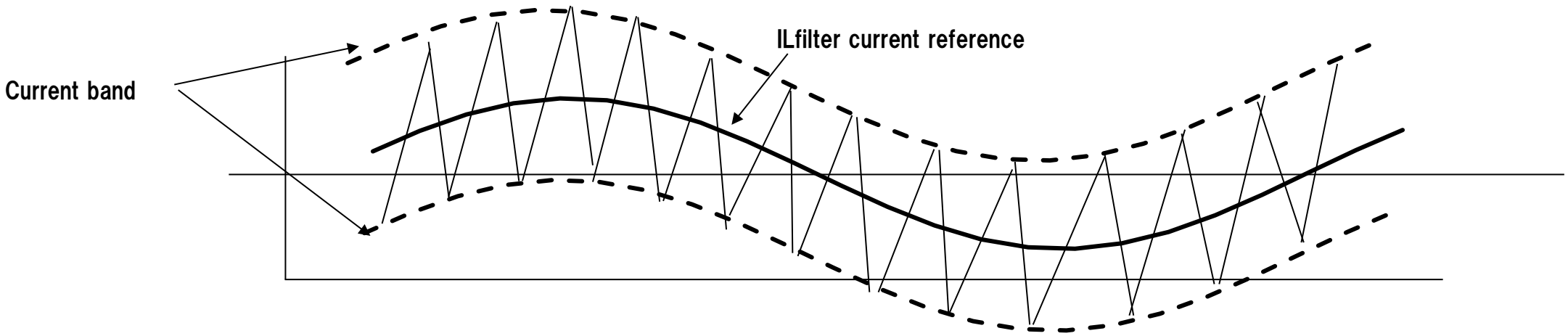
- Set ILfilter current reference
- Set Current band (can be wide)
- Vfilter=1/Cfilter* ∫ ICfilter dt

Hysteresis mechanism

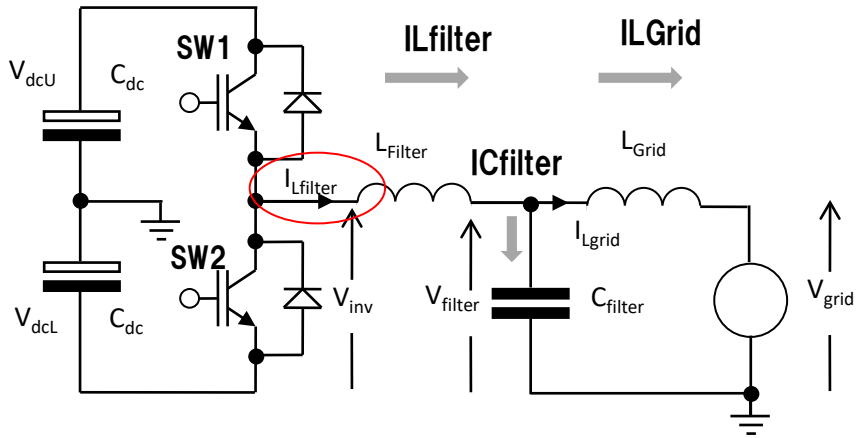
- Sw1 ON until ILfilter measured exceeds upper current band
- Sw1 OFF and Sw2 ON until ILfilter measured exceeds lower current band
- Sw1 ON and Sw2 OFF and repeat

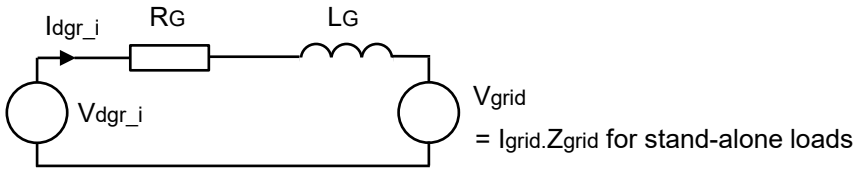
Advantage

- Current measurement with wide band will be accurate



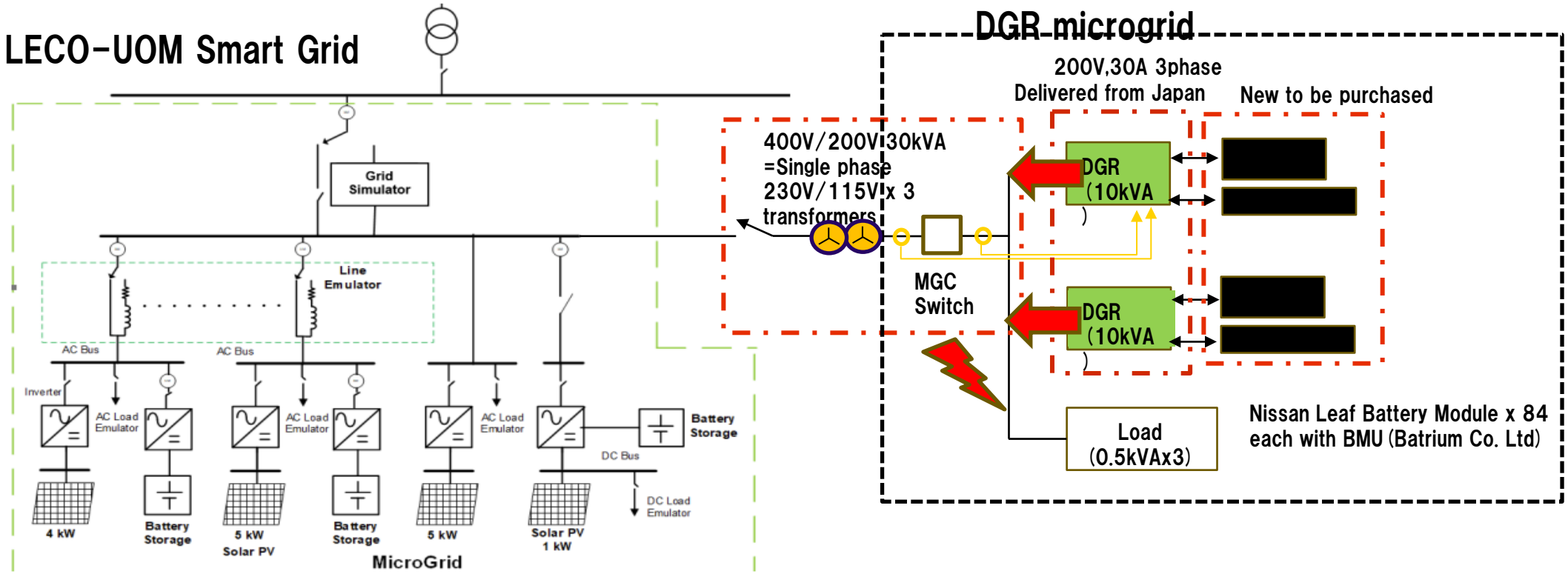
(5) Grid Connect Inverter





- **Connect Half Bridge Inverter to the Grid**
  - L_{Grid}: Grid inductance: DGR standard connection to the Grid
  - IL_{Grid} = (Vgrid−Vfilter) /Lgrid
  - IL_{filter} = (Vfilter−Vinv) /Lfilter
  - IC_{filter} =ILgrid−Ilfilter
  - Vfilter=1/Cfilter∗ ∫ Icfilter dt
- **Power reference**
  - Pgrid =Vgrid∗ILgrid∗cos ϕ
  - Qgrid =Vgrid∗ILgrid∗sin ϕ
  - Control ILgrid and ϕ
  - ILgrid is not controlled directly by PWM voltage control
  - PWM control is difficult the current, because it control Vfilter
  - Then differential of Vfliter and Vgrid makes ILgrid
  - When Vgrid changes, ILgrid changes largely and cannot control
- **Direct Control of current by Hysteresis: Patented**
  - ILgrid=ILfilter+Icfilter (Icfilter≒0)
  - Then ILfilter≒ILgrid
  - DGR controls ILfilter directly.

DGR Mini Grid Short Circuit Test:
Fault Current suppressed and restore smoothly: Succeeded



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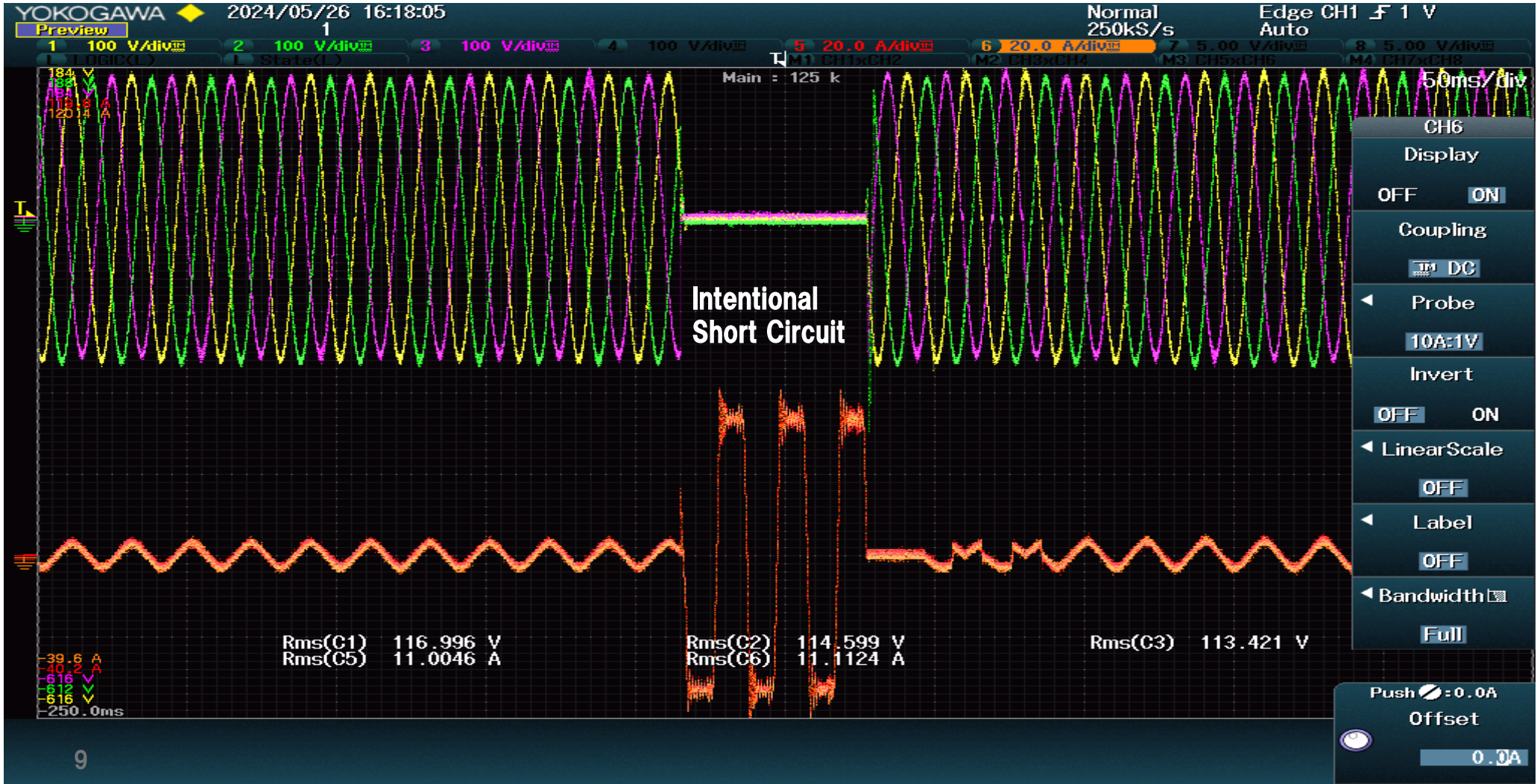
(6-1) Short Circuit

DGR Mini Grid Short Circuit Test:
Fault Current suppressed and restore smoothly: Succeeded



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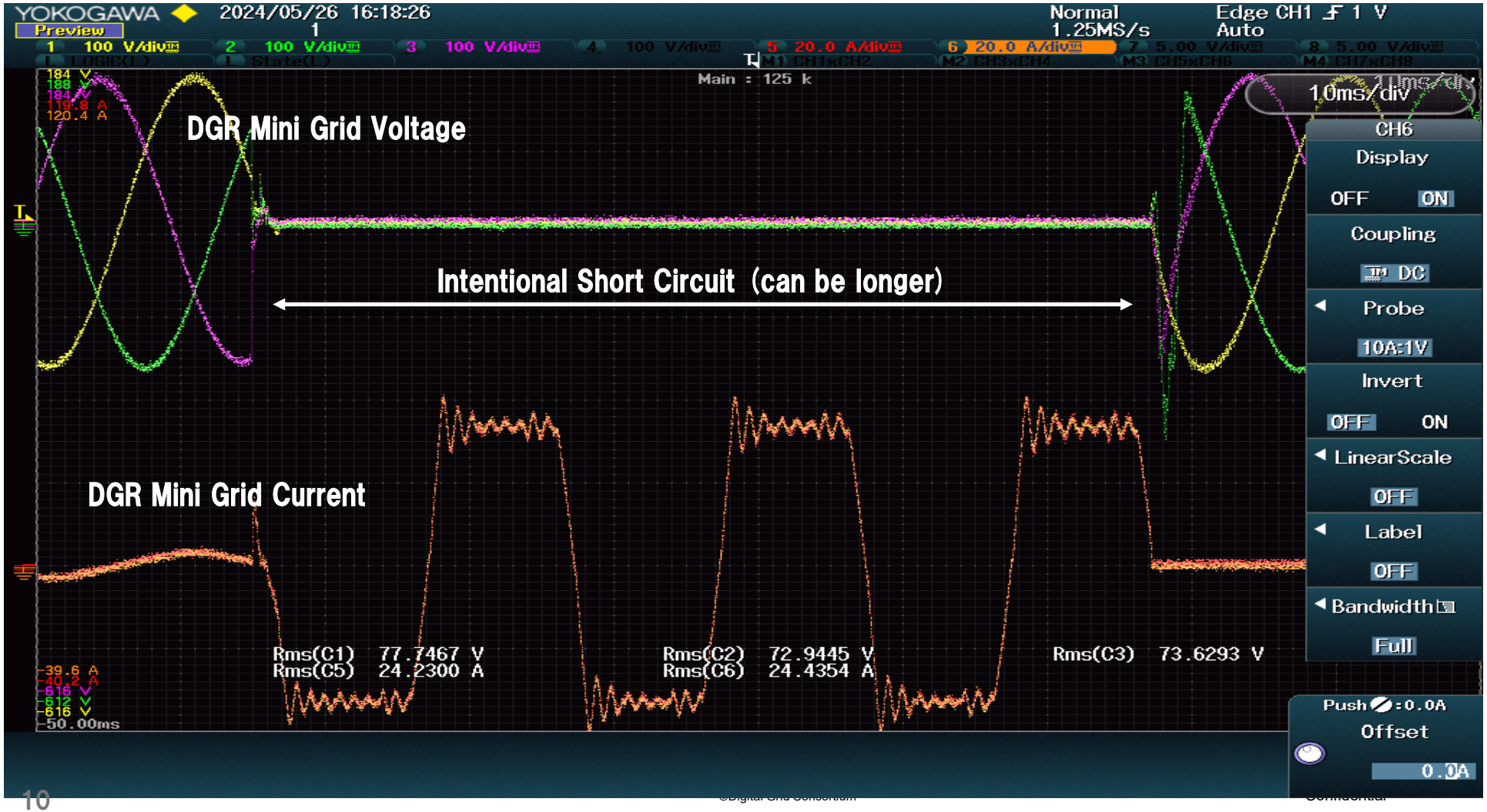
(6-2) Short Circuit

DGR Mini Grid Short Circuit Test:

Fault Current suppressed and restore smoothly: Succeeded



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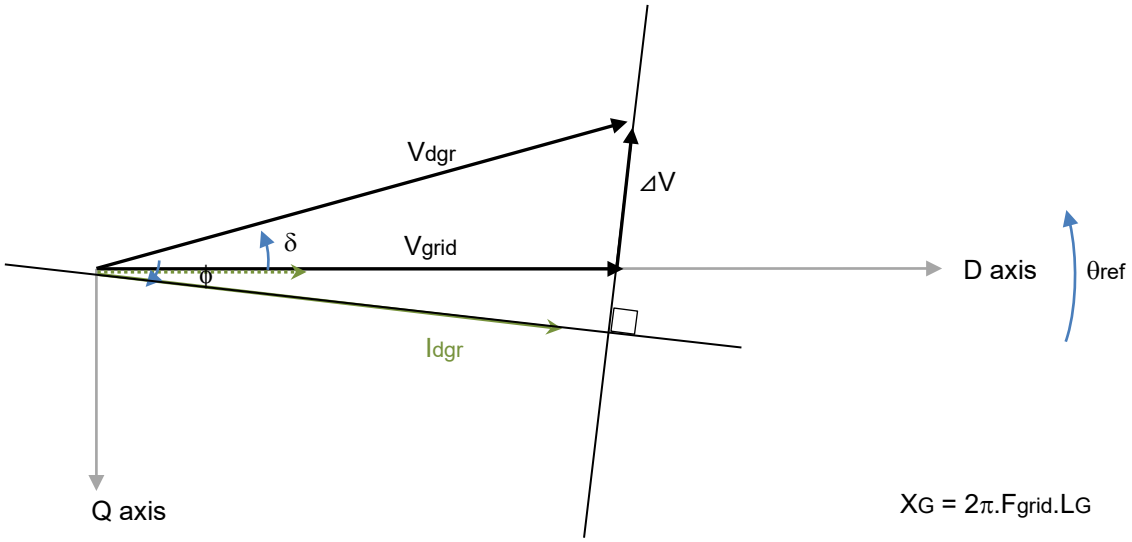
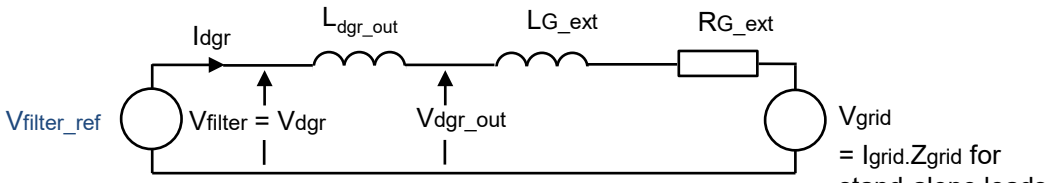
2. Grid Following and Grid Forming Concept

(1) Grid Following (GFL)



$X_G = 2\pi.F_{grid}.L_G$

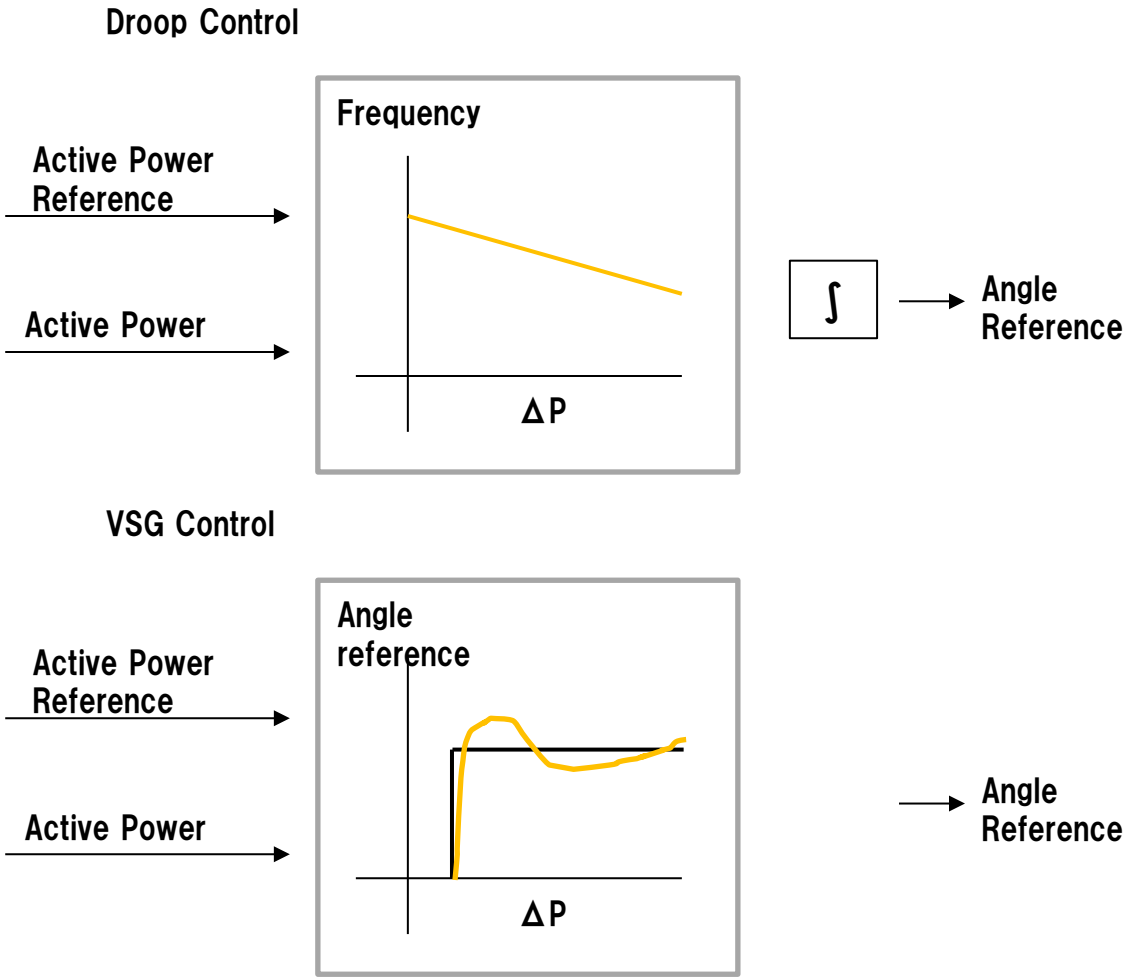


VLdgr_out = Vdgr – Vdgr_out
(Inductor voltage measurement or estimate)

- **Current Source**
  - Vfilter=Vdgr
  - ΔV=Vgrid-Vdgr (vector)
  - Idgr is determined by ΔV and L_G
  - Cos ϕ is usually set to 0.9 to 1.0
  - Smart inverter is required to change cos ϕ
- **Idgr is controlled by Vdgr**
  - Current source is controlled by voltage
  - Voltage is controlled by PWM
  - Slow to Vgrid change
  - Cannot control short circuit current
- **Power flow constant**
  - P=Vgrid*Idgr*cos ϕ
- **Do not supply Inertia**
  - When Vgrid changes Idgr keeps P
  - It does not supply Inertia (=Additional P injection or absorption)

2. Grid Following and Grid Forming Concept

(2) Grid Forming (GFM)



Two major GFM concepts

- "Droop Control" with Frequency and Voltage and "VSG" which is Virtual Synchronous Generator

Droop Control with Frequency and Voltage

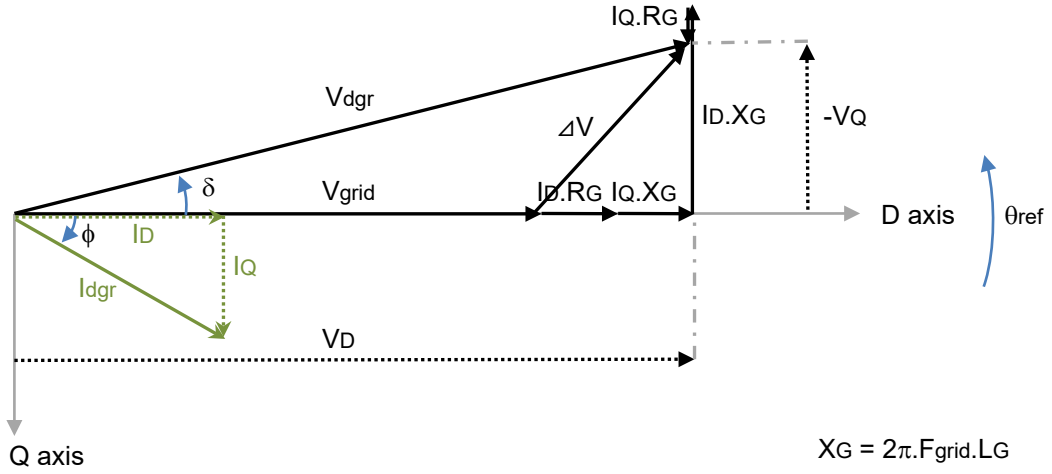
- When grid frequency changes, change the output of GFM inverter
- Integral may not be allowed, because it affects main grid operator control
- Droop control is similar to governer control of generators

Virtual Synchronous Generator

- When active power changes, GFM behaves like synchronous generator to cope with real generators
- It may have second order characteristics oscillation equation of synchronous generator
- Different type of equations may affect each other and cause unexpected oscillation of the grid voltage and frequency

2. Grid Following and Grid Forming Concept

(3) DGR's Grid Forming



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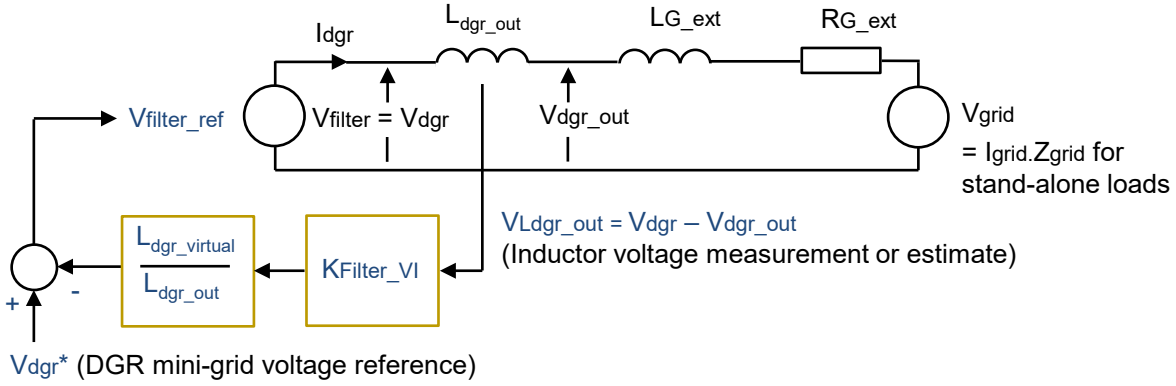


DGR Grid forming is "Grid Impedance Control"

- When DGR starts operation, Vdgr is established
- ΔV is established with the difference of Vgrid and Vdgr
- In the output circuit, physical impedance of R_G and L_G are existing between Vdgr and Vgrid

Idgr is determined by ΔV and physical impedance

- $\Delta V_D = I_D * R_G + I_Q * X_G$: $(X_G = 2\pi f L_G)$
- $-\Delta V_Q = I_D * X_G - I_Q * R_G$

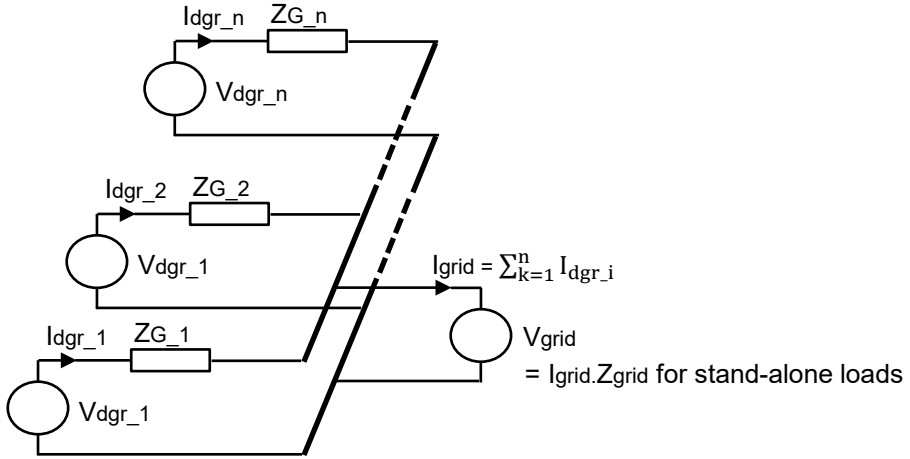
Virtual Impedance

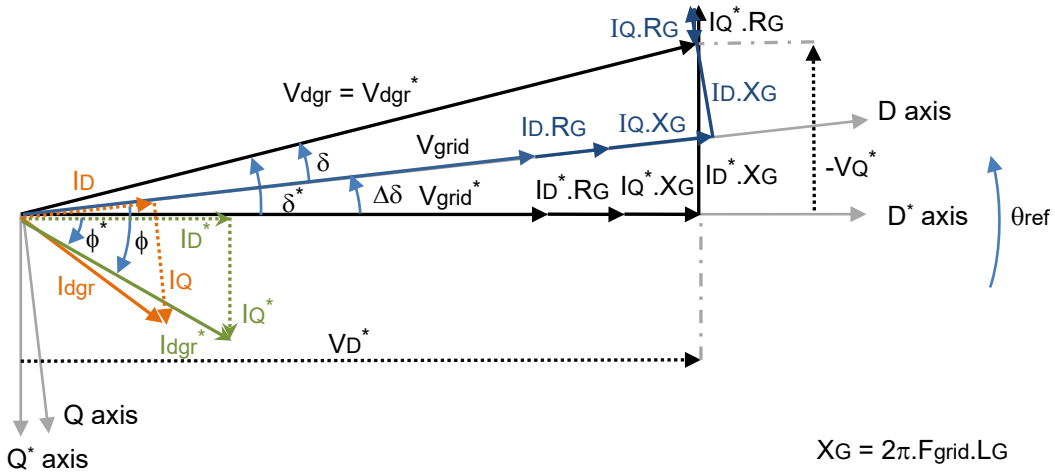
- DGR uses virtual impedance to add in the calculation
- Total impedance is almost equal to generator grid impedance
- When the output impedance is similar value, load sharing and active, reactive power balance is almost even with grid and DGR
- We can change the balance of load sharing and power flow by angle addition

Virtual Inertia

- When the grid voltage or frequency changes suddenly, Vdgr maintains the magnitude and angle for short time.
- Then ΔV changes because of Vgrid change.
- Idgr instantly supply or absorb the active and reactive power

(1) Grid Connected: Voltage synchronization by PLL





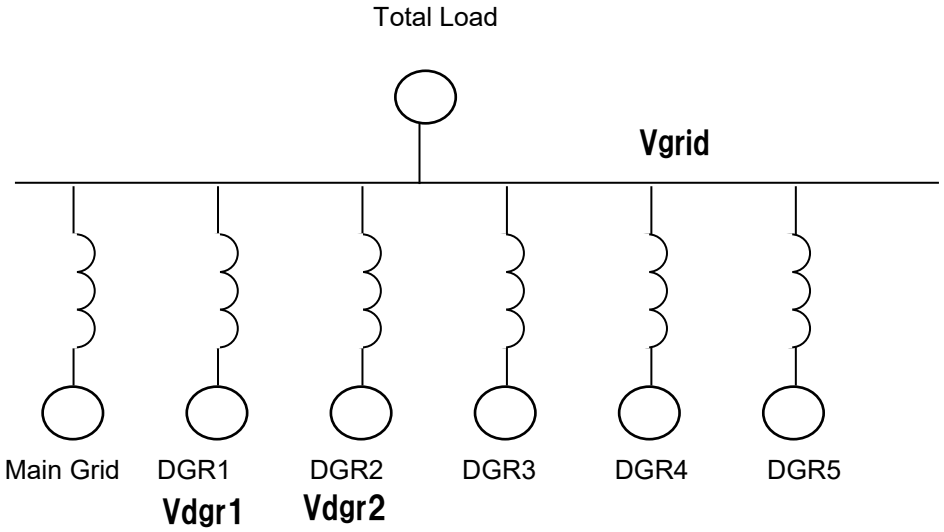
XG = 2π.Fgrid.LG

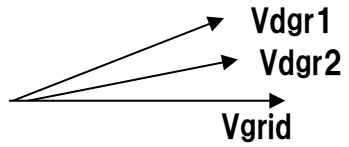
Grid Connected

- Grid is very robust
- PLL finds Vgrid which is common to all the DGR
- Each DGR control Vdgr so that Idgr and ΔV settles designated virtual impedance

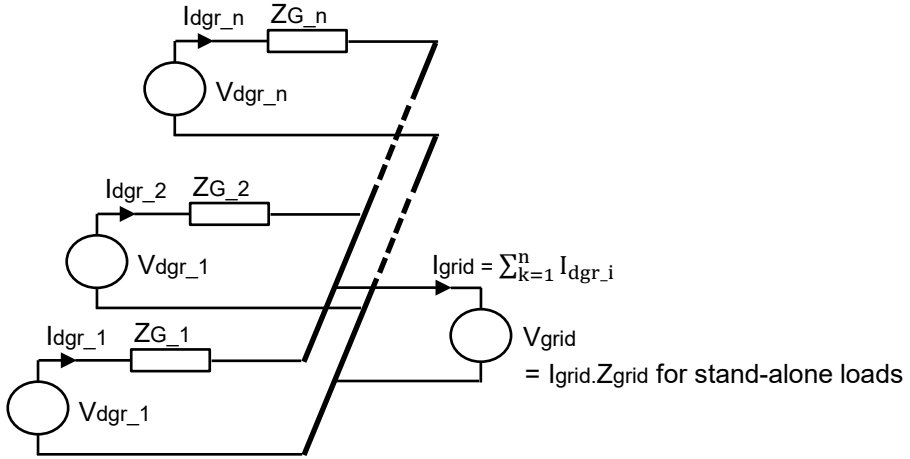
Synchronization

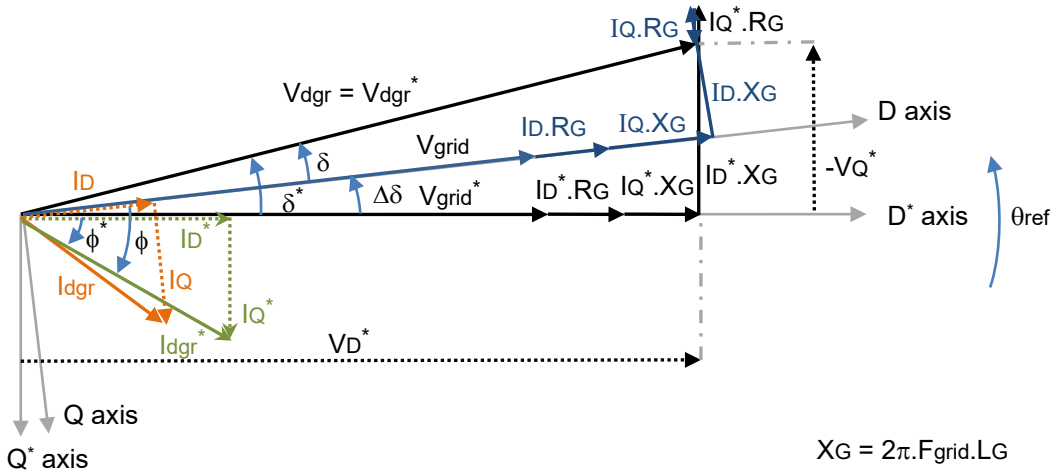
- When Vdgr1 and 2 different, they adjust to make a virtual impedance to setpoint





(2) Grid Disconnected: Voltage synchronization by PLL



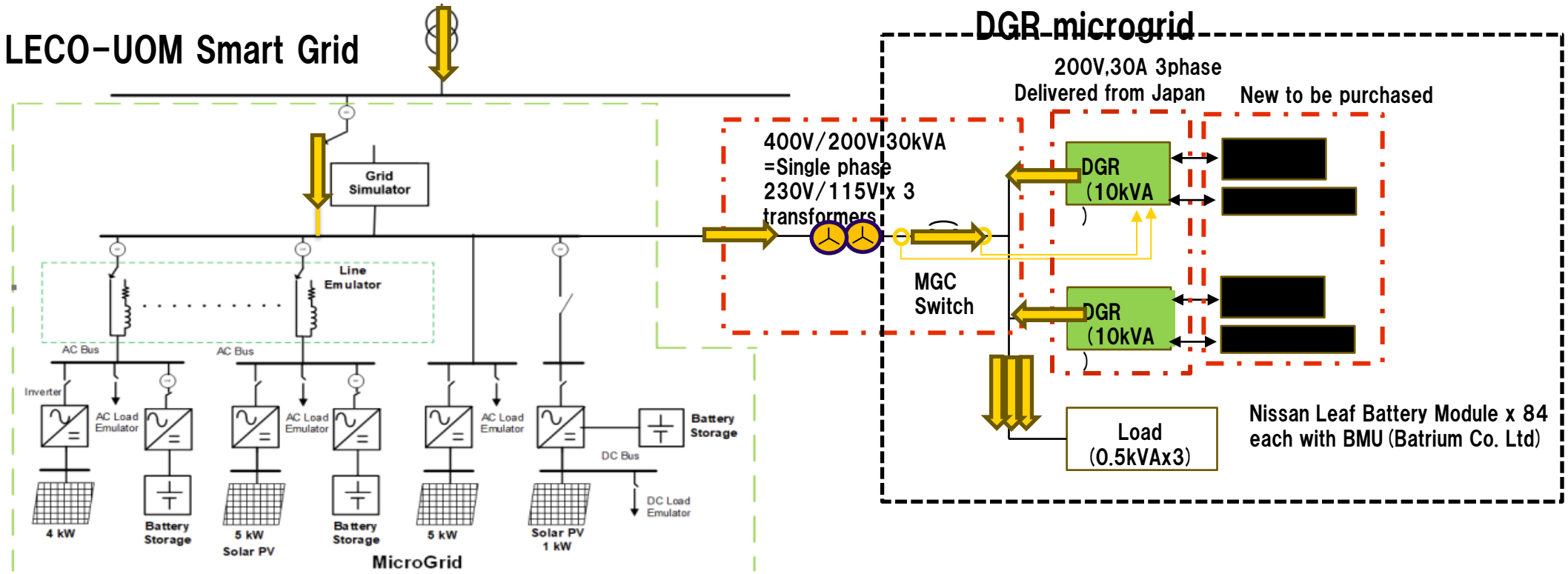


$X_G = 2\pi.F_{grid}.L_G$

- **Grid Disconnected**
  - Grid is very robust but disconnected
  - PLL finds Vgrid which is developed by DGR
  - Each DGR control Vdgr so that Idgr and ΔV settles designated virtual impedance.
  - However, there is a positive feedback loop and unstable
- **To make it stable, special control is required**
  - Frequency reference is set to 50Hz
  - Difference of frequency is controlled by PI control
  - It is important to apply suitable parameters
- **Then independent operation can be established**
- **When main grid become available, synchronizing technic is adopted via cloud ϕ global control**

Implement small scale grid forming microgrid test: Succeeded

- ✓ Direct Connection to the LECO Main Grid
- ✓ Two DGRs work together and share the load with Main Grid at 1:1:1 ratio.
- ✓ Independent operation of two DGRs are succeeded
- ✓ Short circuit test is conducted, and the fault current is limited



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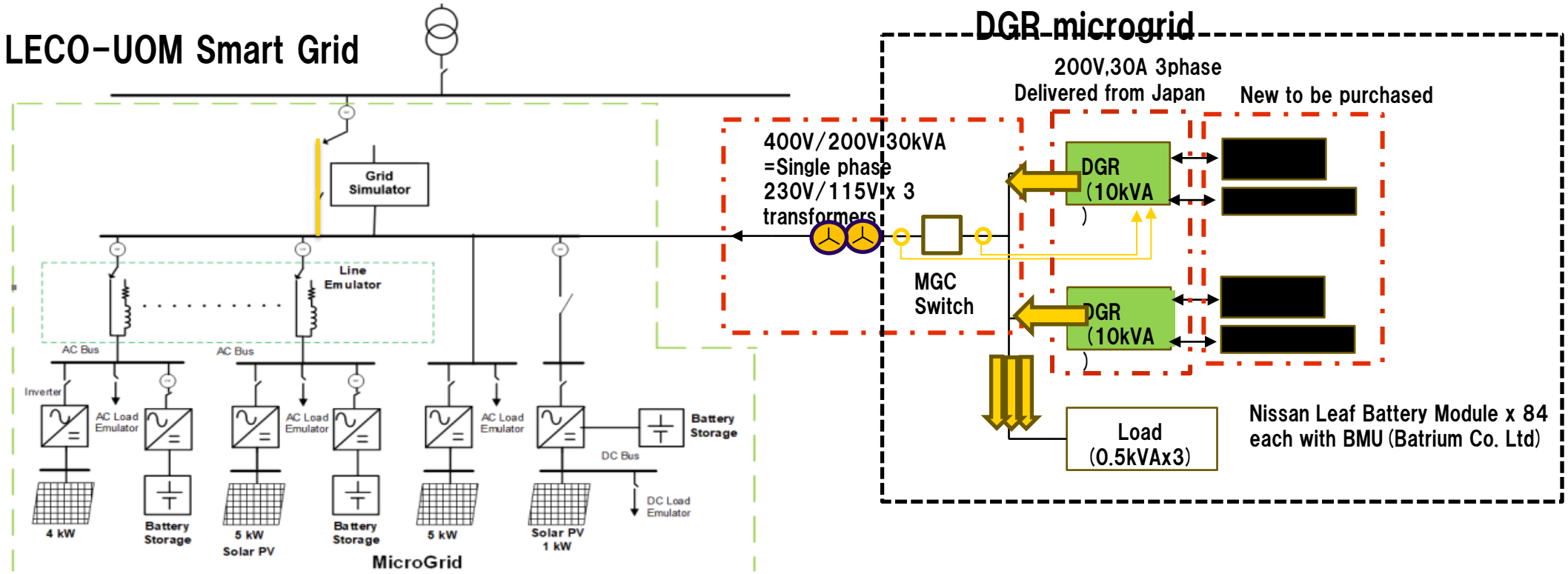

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Implement small scale grid forming microgrid test: Succeeded

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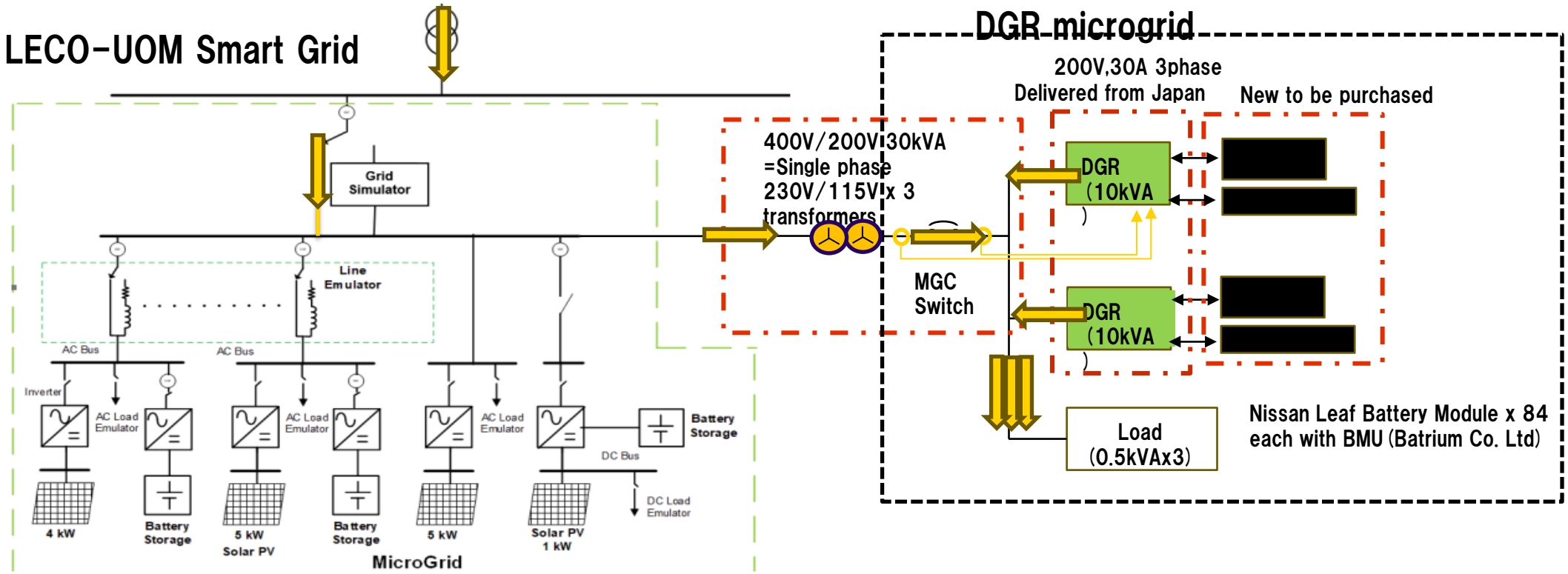

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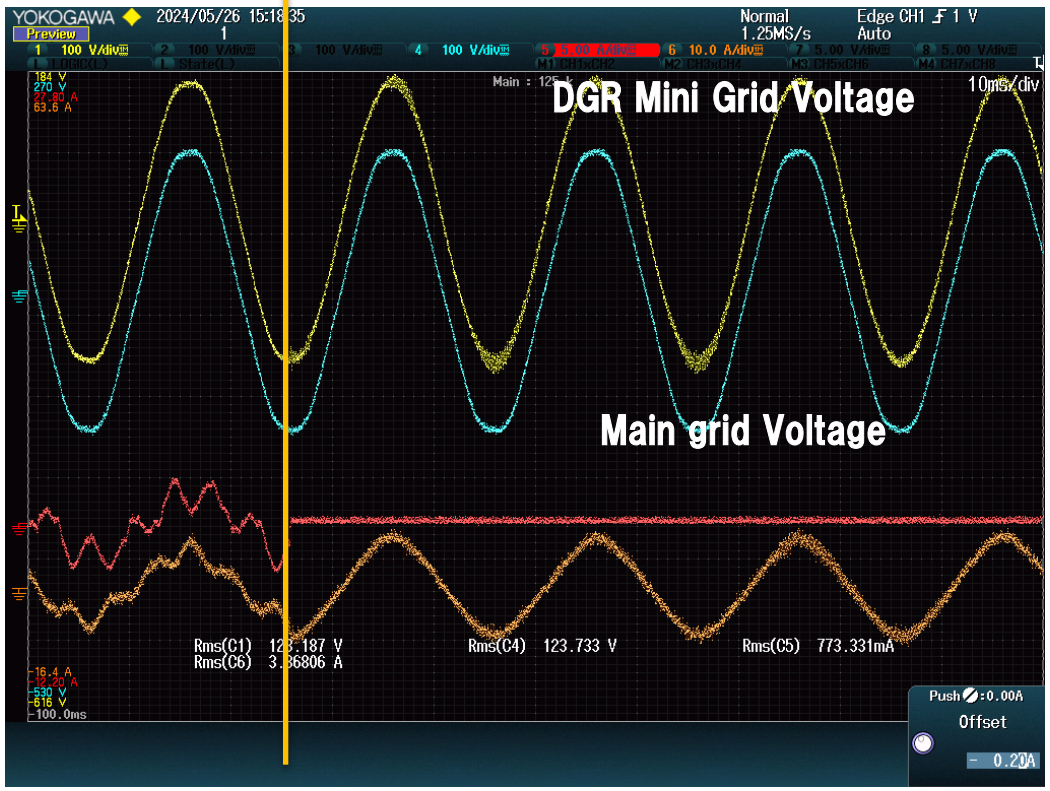
Load sharing

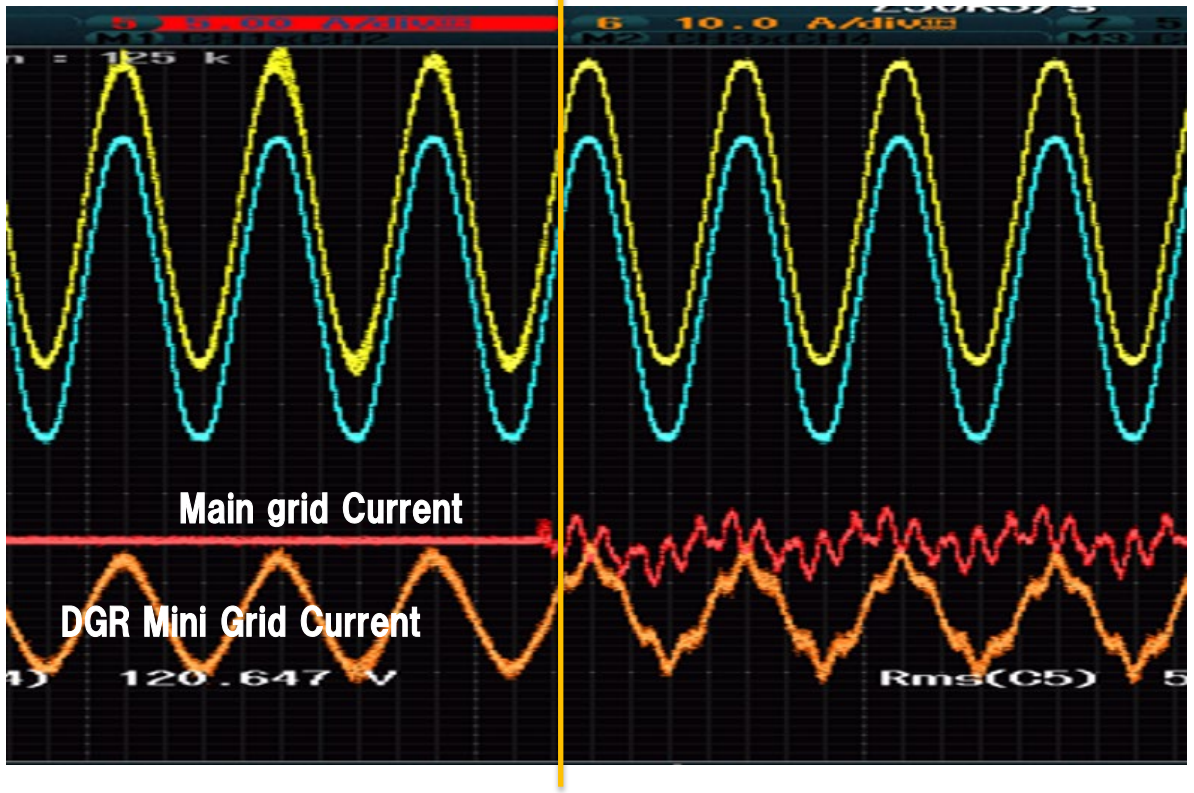
Main Grid – DGR Mini Grid Disconnect/Connect test

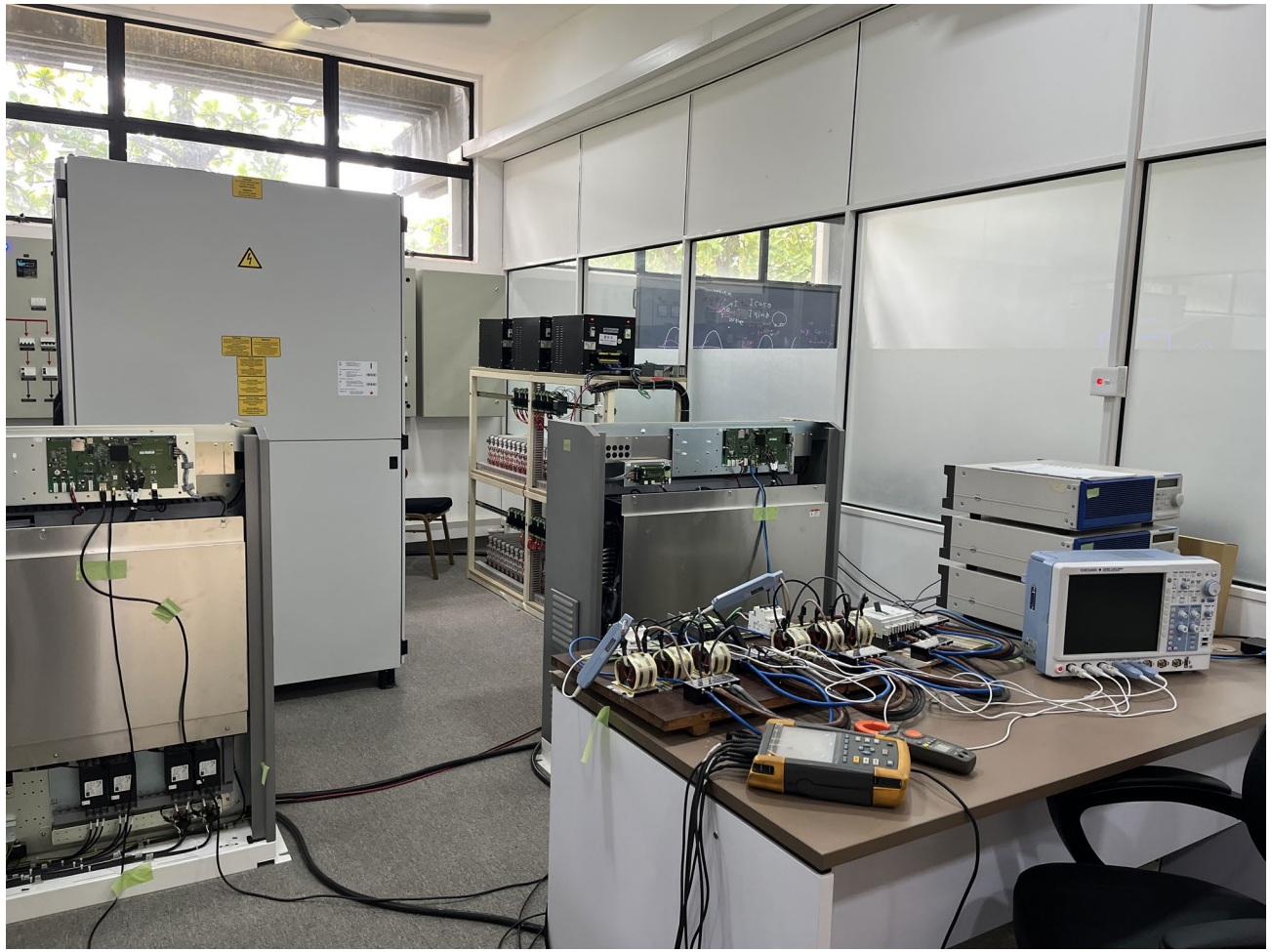
Connect

Disconnect

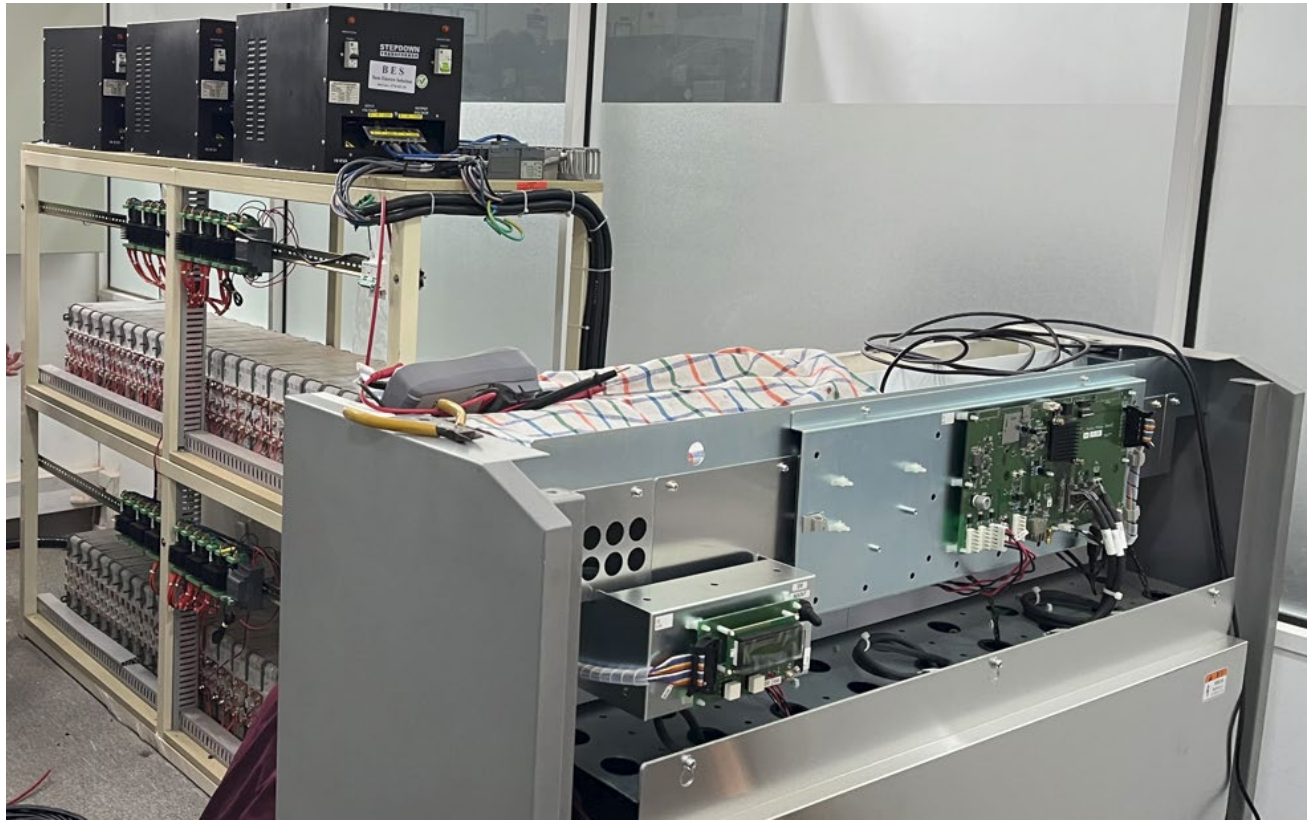
Reconnect





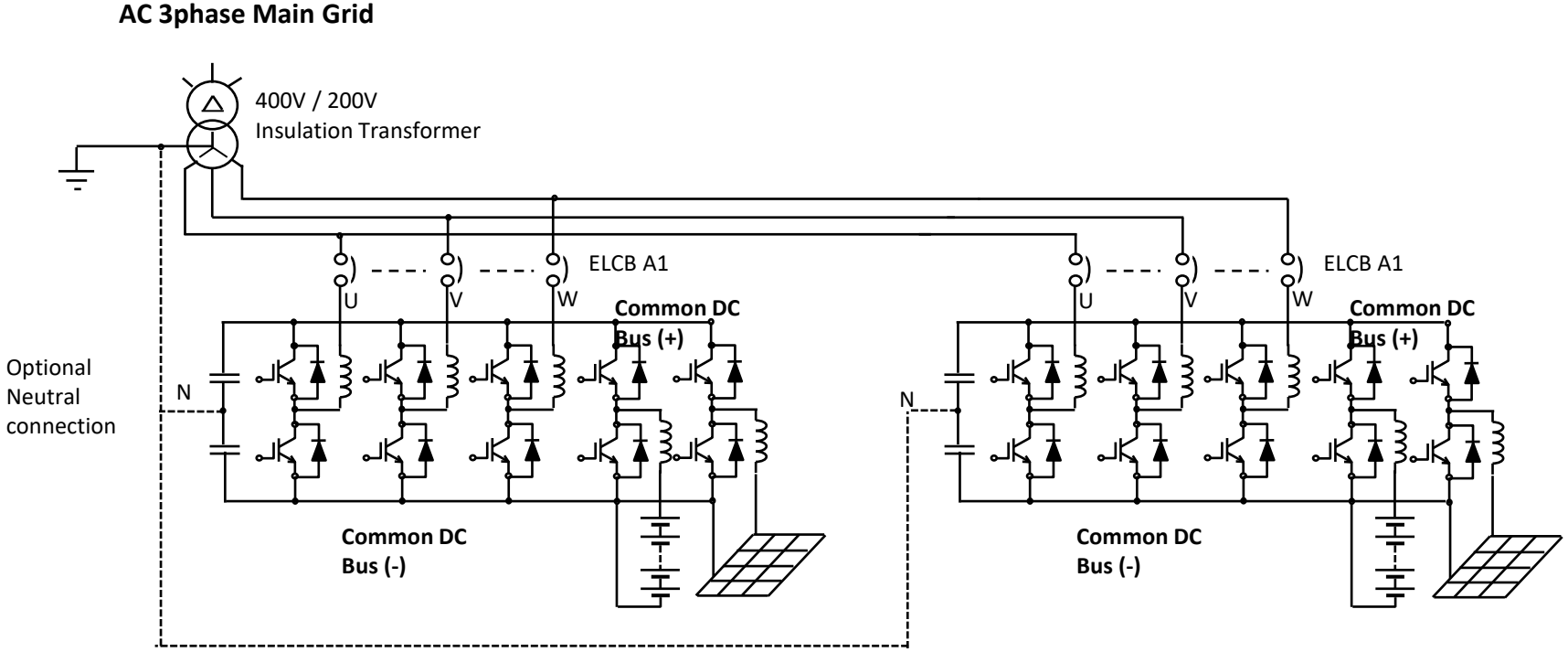


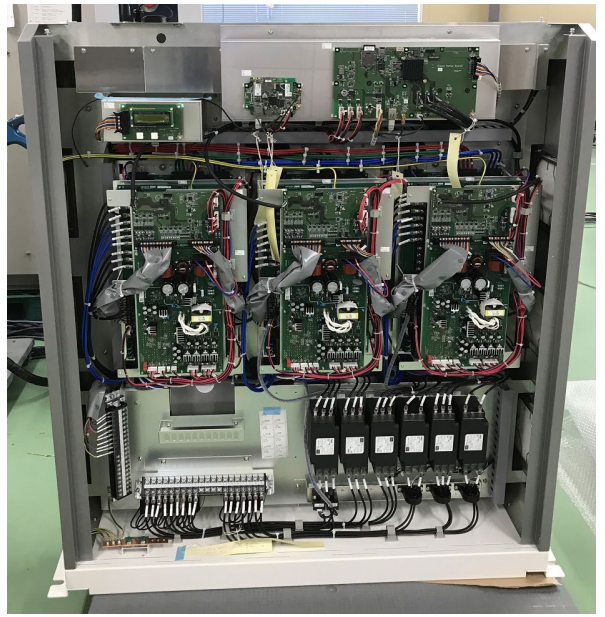
Newly Installed Digital Grid Research Lab

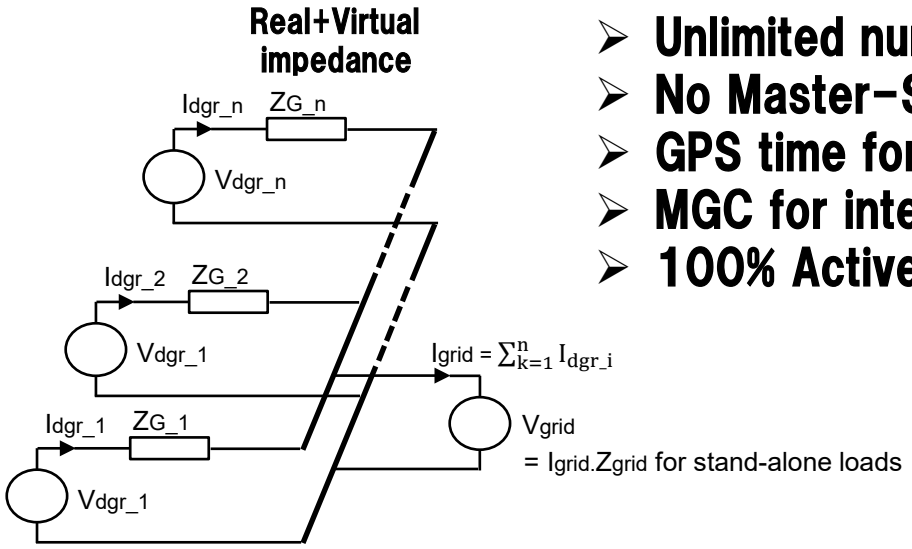


DGR Micro Grid

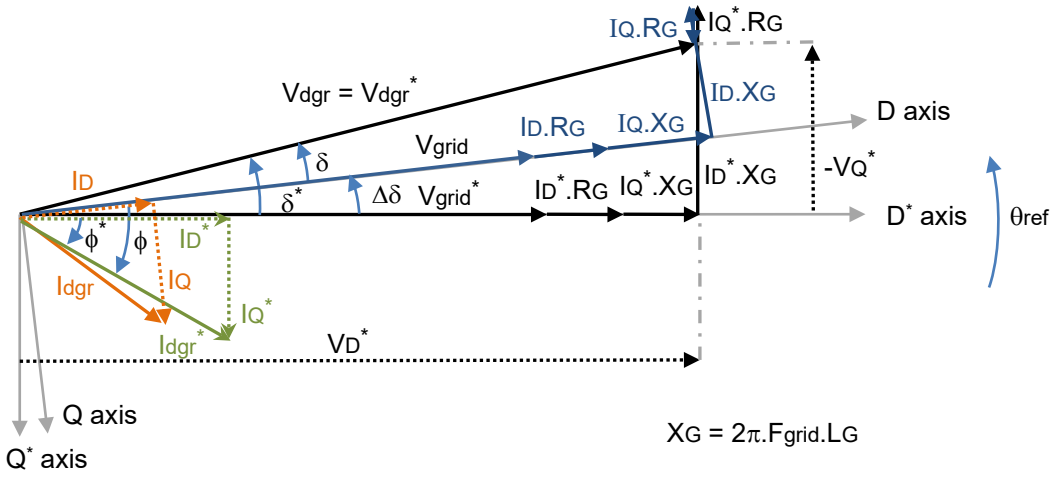
- Multi-leg half bridge inverters with common DC bus
- Gate pulse control AC and DC power units
- AC output operates on Grid Forming Mode
- Number of AC output synchronize using virtual impedance

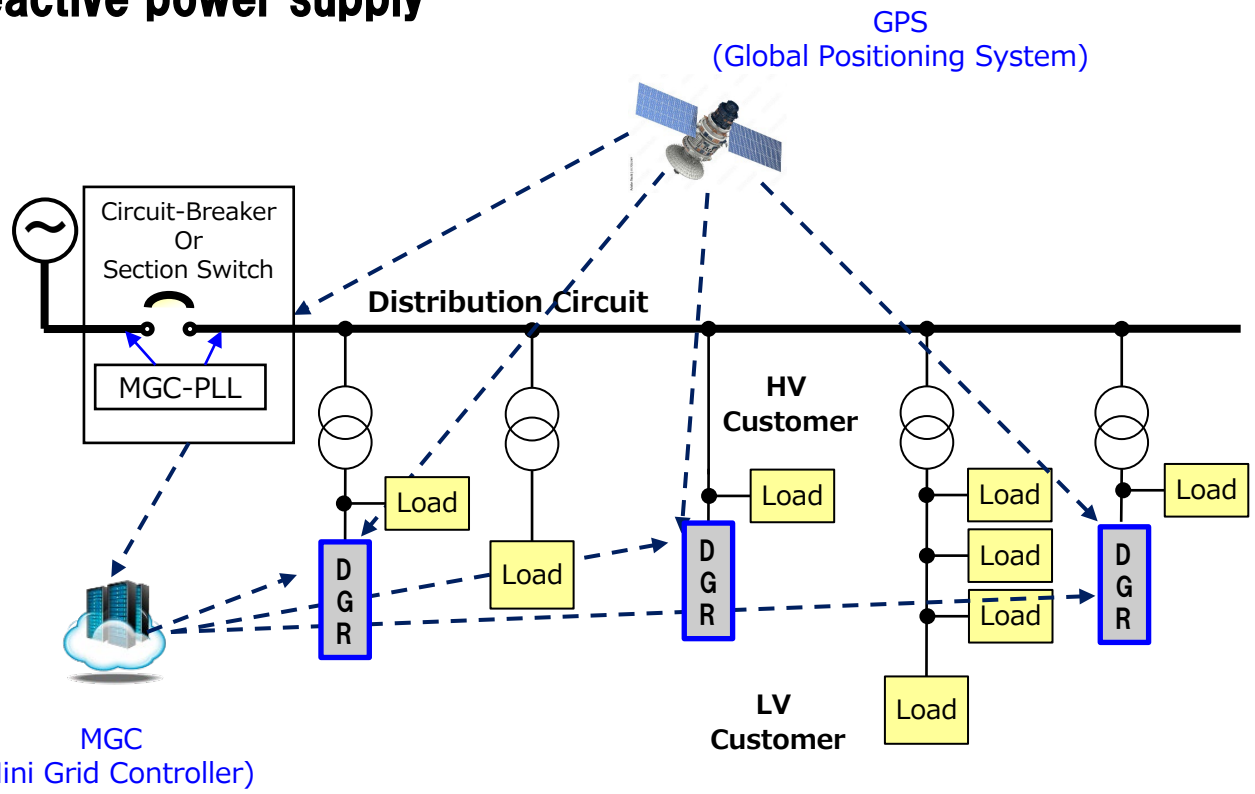




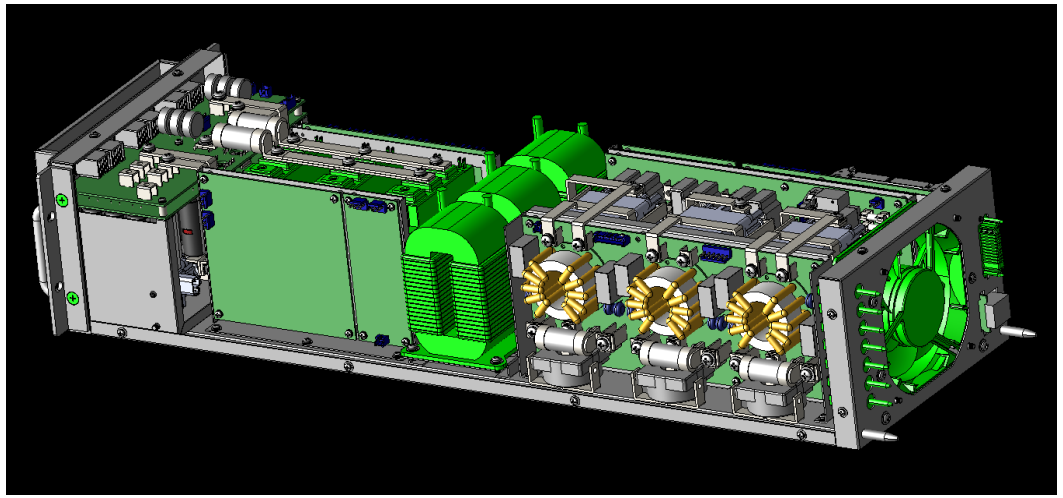


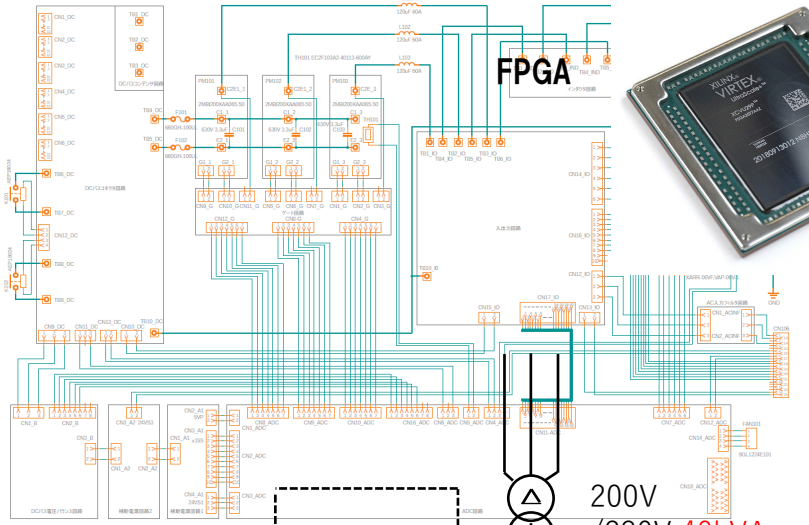
- **Unlimited number of DGRs synchronize**
- **No Master-Slave mechanism**
- **GPS time for Black Start**
- **MGC for intentional power flow**
- **100% Active/Reactive power supply**





20kW Helios Unit





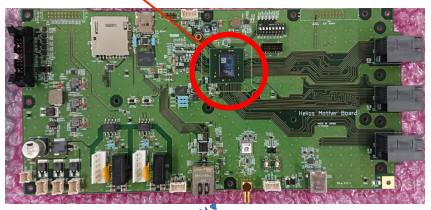


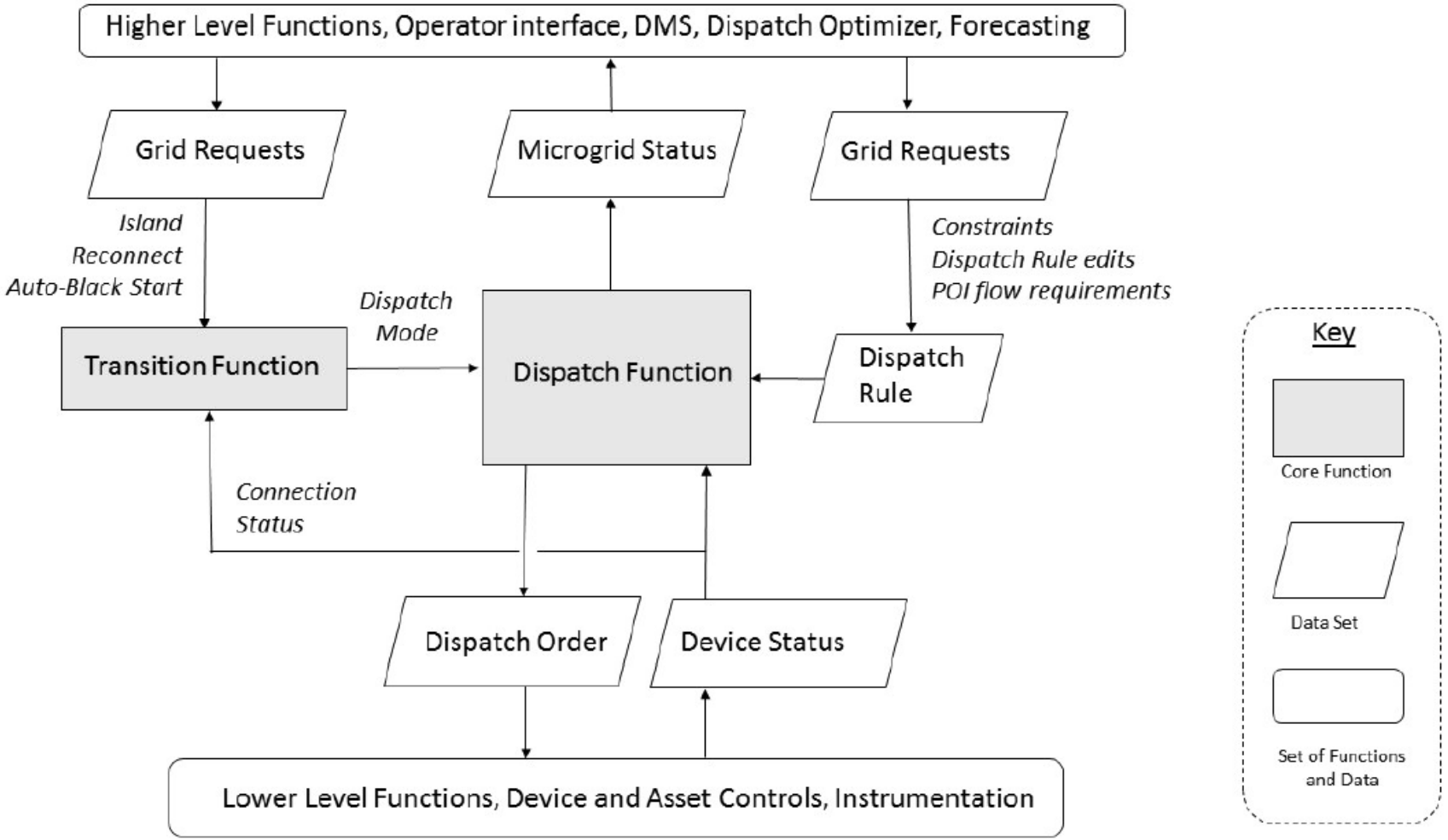
table 2. The summary of the requirements and additional capabilities recommended for GFM inverters.

	GB Grid Code	AEMO	European Union Grid Code (Draft)(**)	UNIFI
Requirements				
Active phase jump power	✓	✓	✓(A)	✓
Active damping power	✓	✓	✓(A)	✓
Voltage jump reactive power	✓	✓	✓(A)	✓
Fast fault current injection	✓	✓	✓(A)	✓
Voltage source behavior	✓	✓	✓(A)	✓
Frequency domain response	✓	✓		✓(*)
Inertial response	✓	✓	✓(High frequency: B) ✓(Low frequency: C)	✓(***)
Last synchronous machine survival	✓	✓		✓
Weak grid operation and system strength	✓	✓	✓(A)	✓
Oscillation damping	✓	✓	✓	✓
GFM within current limits	✓	✓		✓
Additional capabilities				
Headroom and energy buffer		✓	(✓)(C)	✓(*)
Current capability above continuous		✓		✓
Black start capability		✓		✓
Power quality improvement		✓		✓
Stability when current limit reached		✓	✓	✓

Type A: Connection point below 110 kV and maximum capacity of .8 kW or more. Type B: Connection point below 110 kV and maximum capacity at or above a threshold proposed by each relevant transmission system operator (TSO), which is below 1 MW. Type C: Connection point below 110 kV and maximum capacity at or above a threshold proposed by each relevant TSO, which is below 50 MW. Type D: Connection point above 110 kV or maximum capacity at or above a threshold proposed by each relevant TSO, which is below 75 MW.
*Even if not explicitly stated in the document, it can be inferred from the specifications that it is a desirable behavior.
**At the present situation, GFM for type A is possible but not mandatory.
***In North America, this requirement is categorized under "fast frequency response" and not explicitly defined.

- ✓ GFM grid code has been discussing as shown in the left table
- ✓ There are no commercial product that cover all the request
- ✓ **DGR has achieved all the requirement for the GFM inverters**
- ✓ Advanced function for Mini grid and micro grid control is also incorporated

IEEE Power & Energy March/April 2024



Relationship between transition and dispatch functions IEEE2030.7 Applicable

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4. ADB's Pilot Project of Digital Grid Research Lab at University of Moratuwa

- ADB introduces most advanced technology of Digital Grid and a tangible pilot plan for new "Grid Forming Micro-grids with renewable energy".

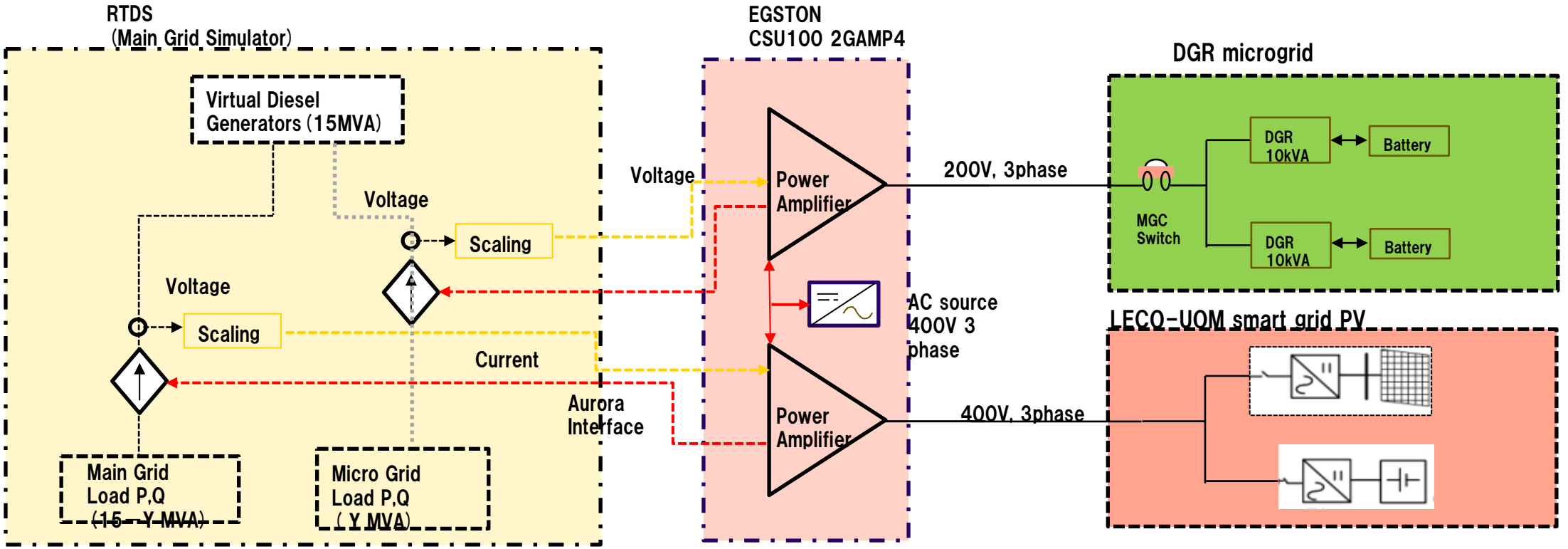
RTDS digital Power Amplifier real DGR

Existing LECO-UOM Smart Grid Research Lab

Newly Installed Digital Grid Research Lab

Implement PHIL test with RTDS-DGR and –Conventional Inverter

- ✓ Conventional Solar inverter and DGR are compared by PHIL test (Power Hardware in the Loop)
- ✓ Conventional Solar inverter may cause the main grid fluctuation
- ✓ DGR grid forming will stabilize the grid fluctuation
- ✓ We will investigate the mechanism and produce the world advance research



28

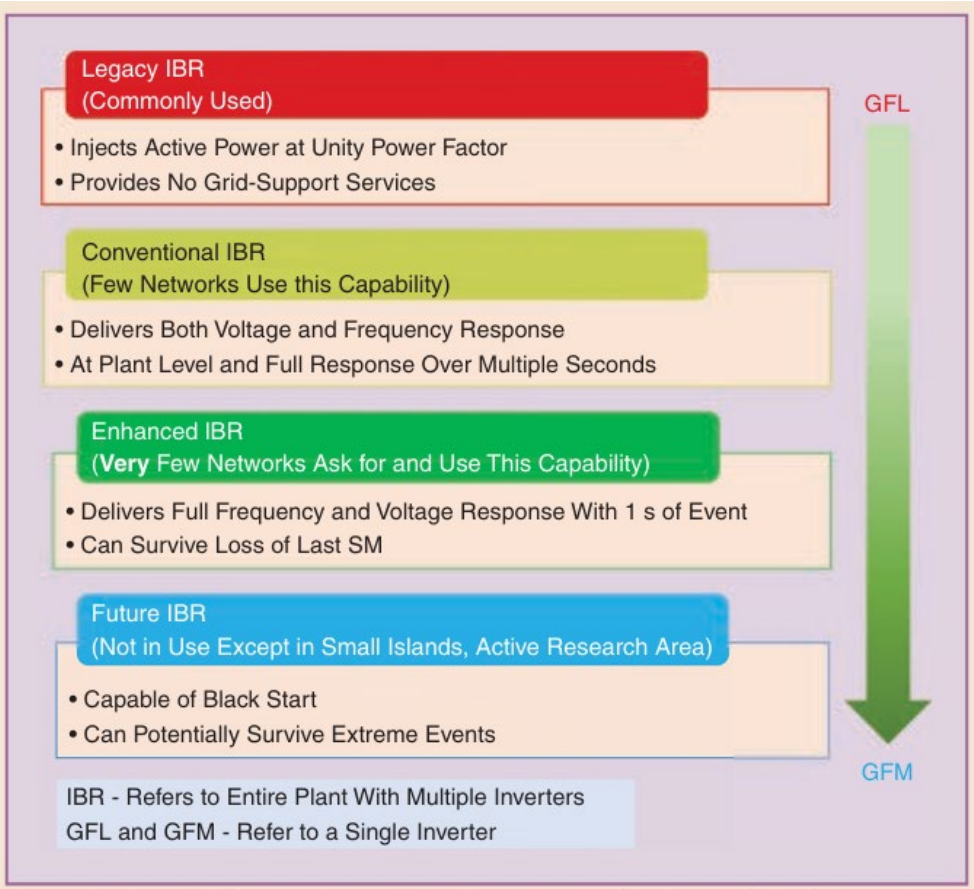
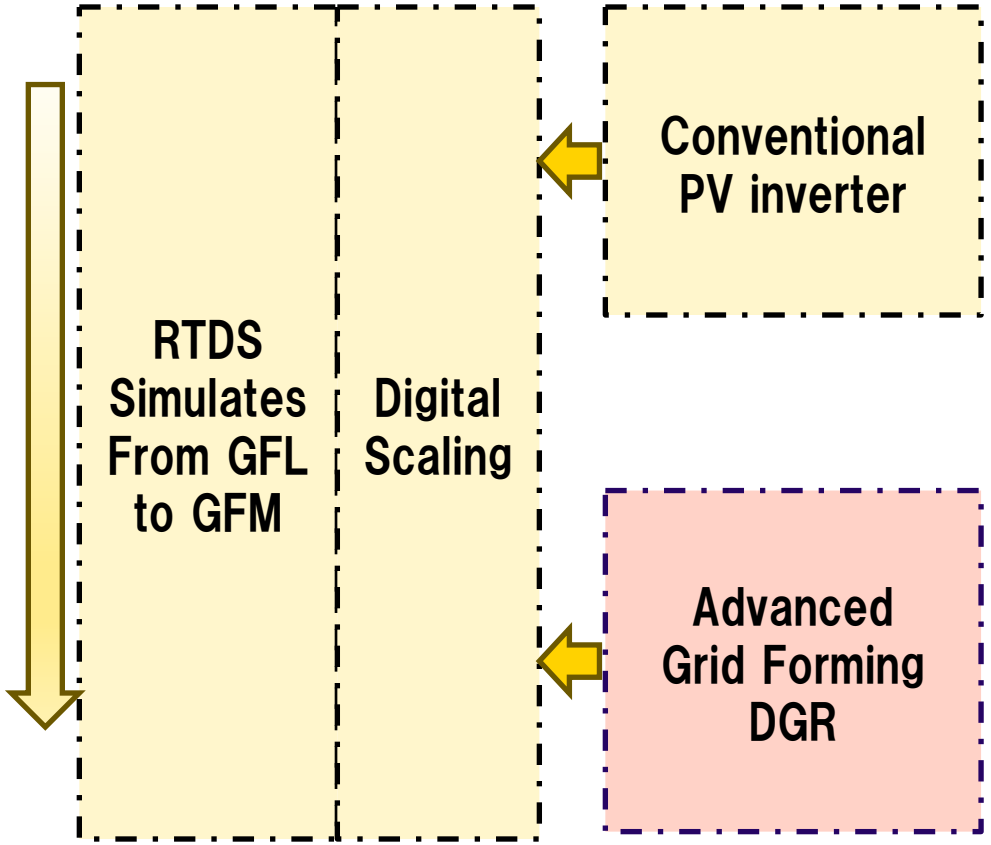


figure S1. Levels of services from legacy, conventional, enhanced, and future IBRs that are utilized in grids around the world and the associated chronology, with an indicative trend from GFL to GFM.



Thank you

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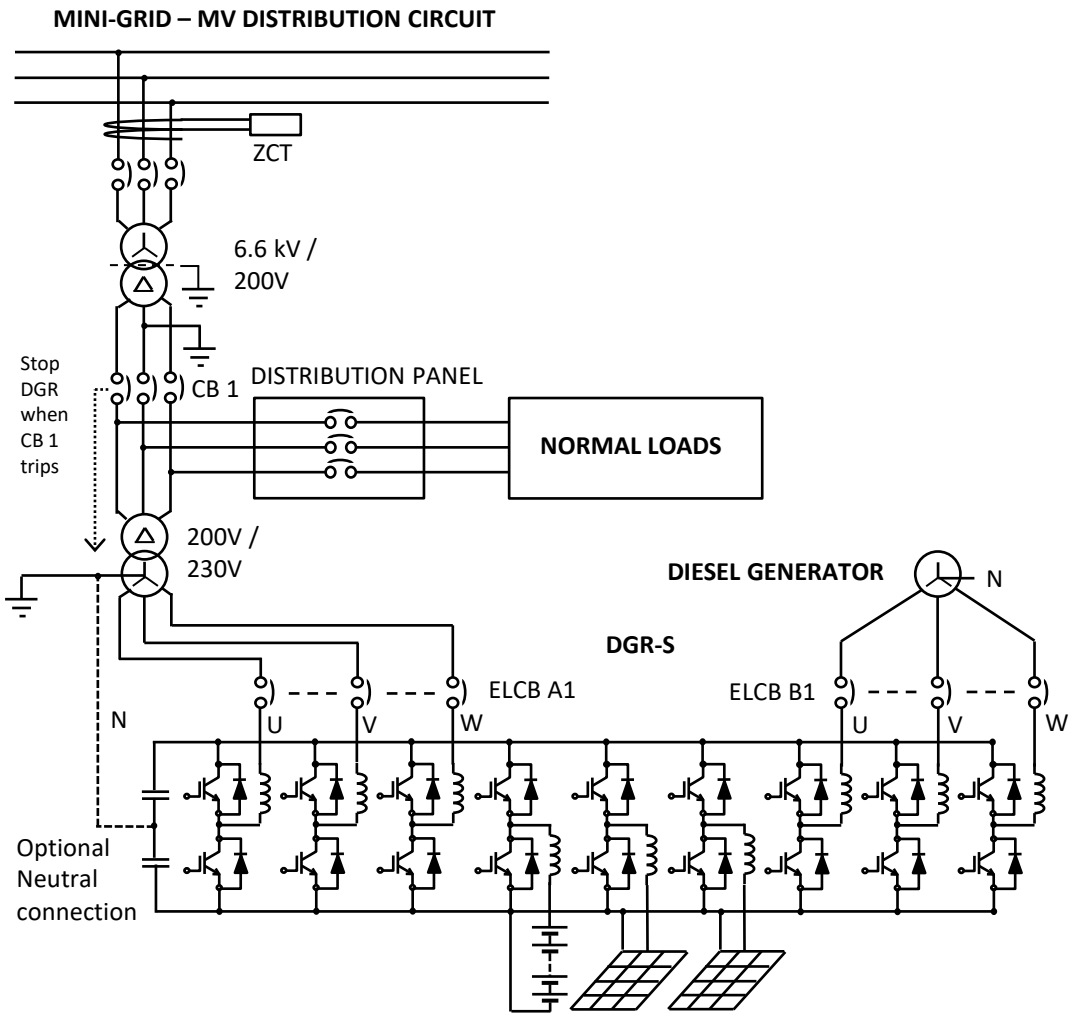
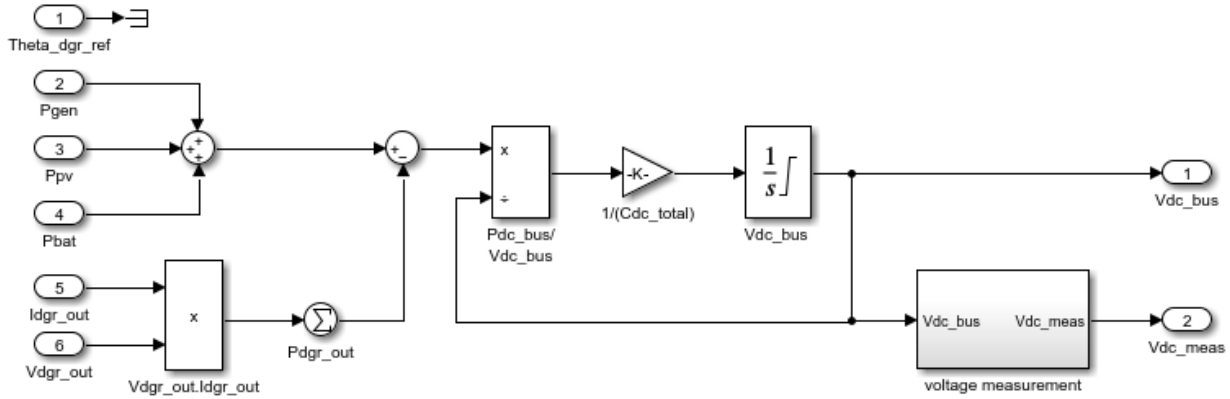
2. DGRの多入力電源制御

(1)DC母線電圧維持制御

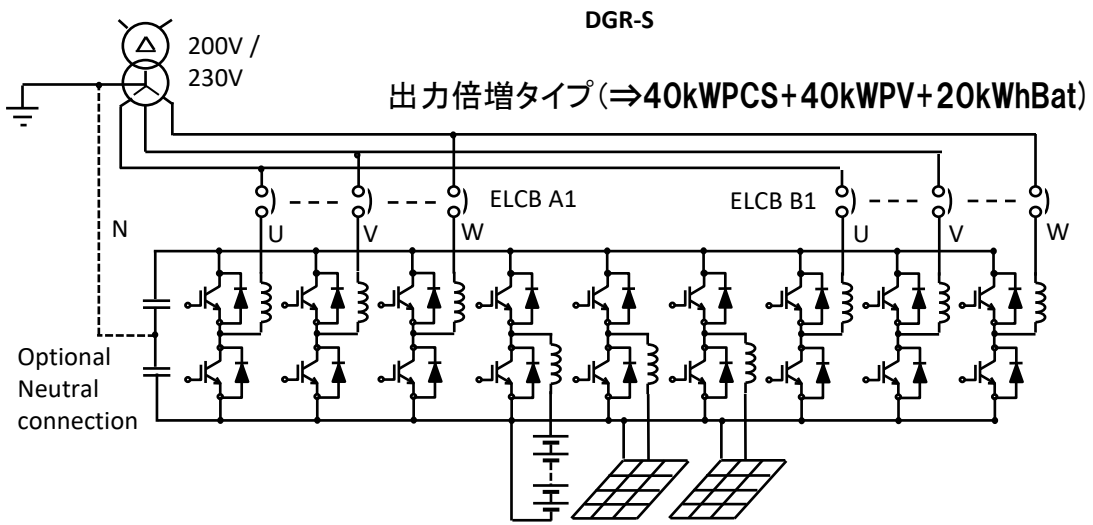


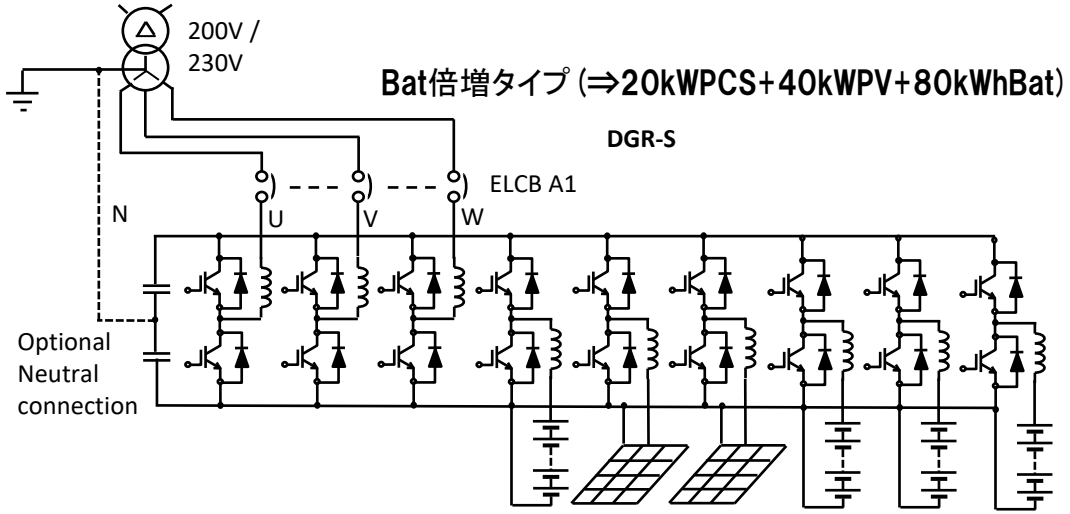
- DGRは他入力電源インバータ
  - 左図は、発電機、太陽光、バッテリーの3入力
  - ハーフブリッヂインバータをレグと呼ぶ
  - 交流入力は3相で3つのレグを使用
  - 交流出力は3相で3つのレグを使用
  - 直流のPVとバッテリーはそれぞれレグを1つとDC母線のマイナス側を使用
- 全電力の差し引き分がコンデンサーに流れ込んで母線電圧を維持する



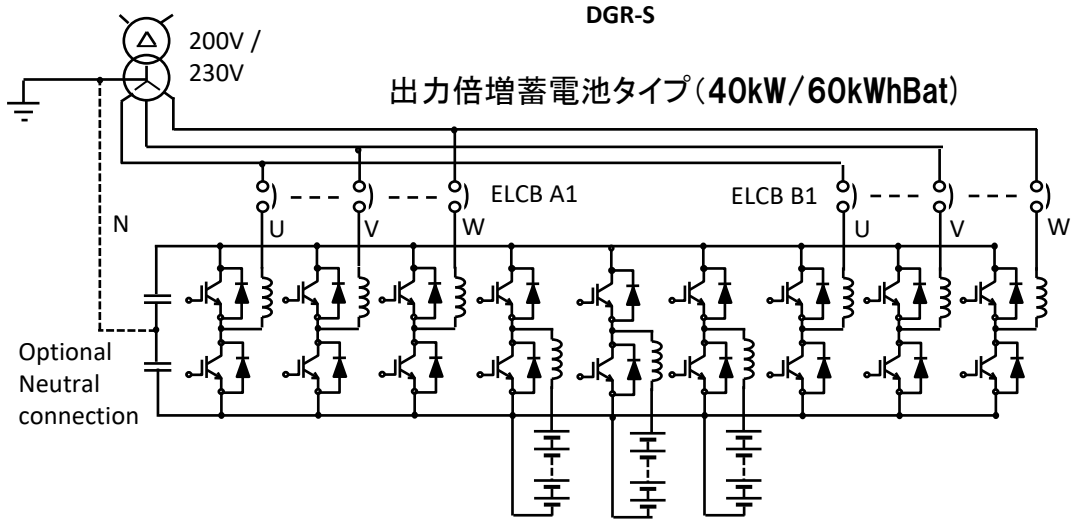
2. DGRの多入力電源制御

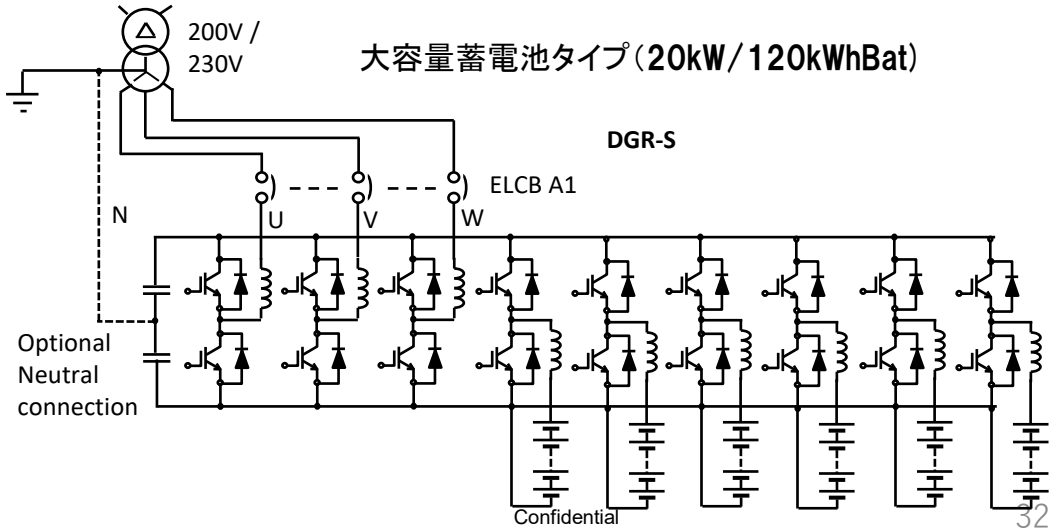
(2)PV/Gen/Batなどマルチ電源の入力制御



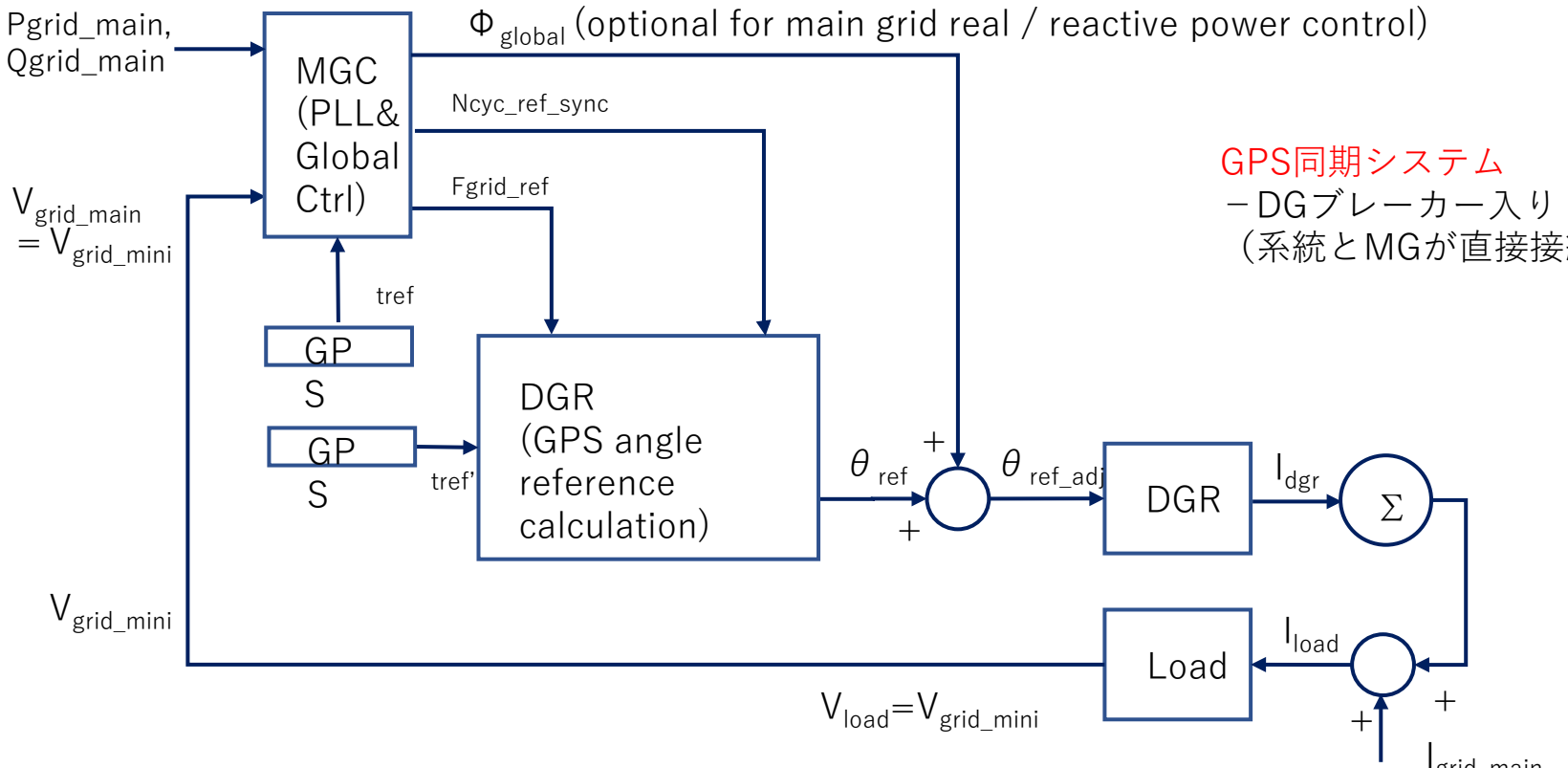


レグの使い方で太陽光パワコンとして出力を倍増することも、蓄電池とのハイブリッドも蓄電池だけで大容量化することも柔軟にできる。

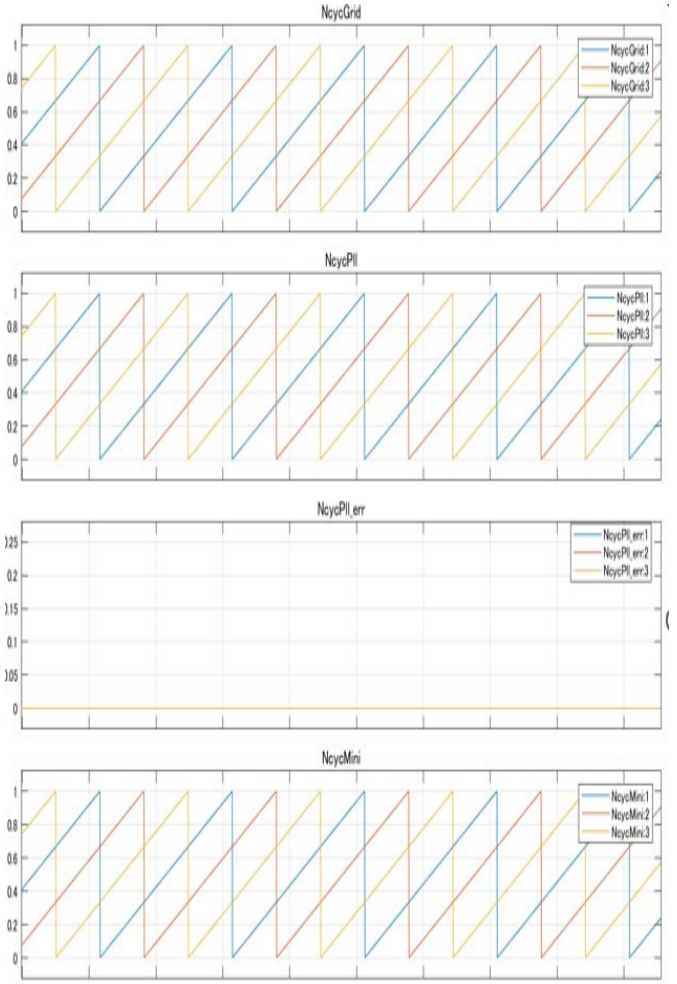




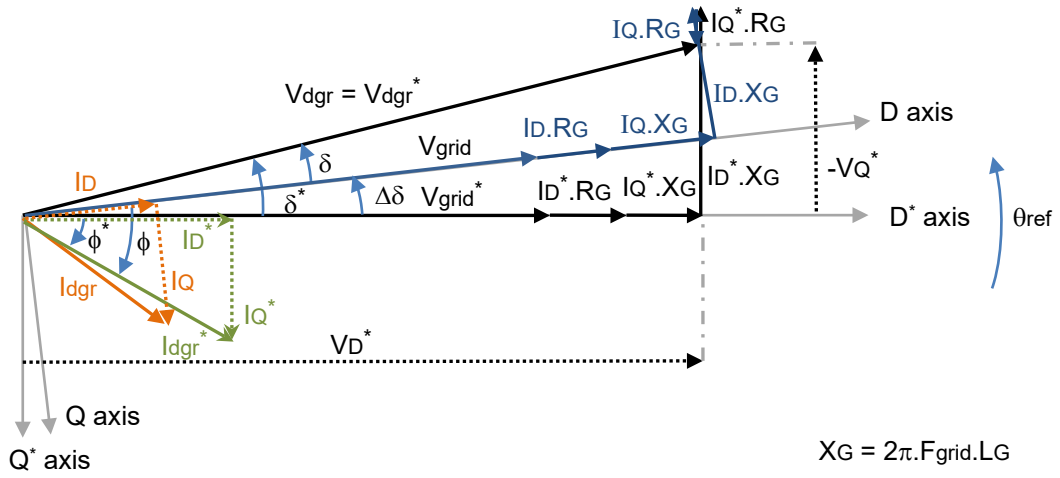
(4)MGC(ミニグリッドコントローラ)による系統位相の伝送



GPS同期システム
－DGブレーカー入り
（系統とMGが直接接続）

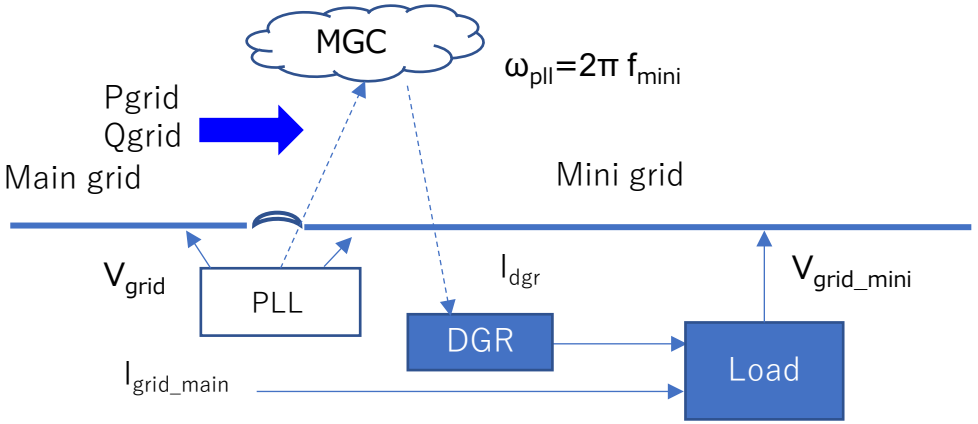


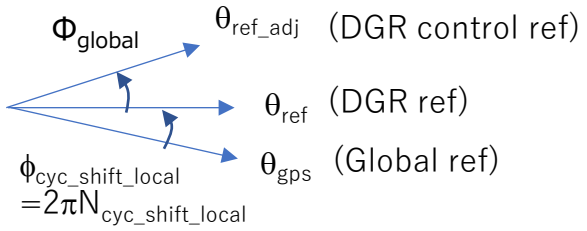
(1)有効電力・無効電力潮流制御



$X_G = 2\pi.F_{grid}.L_G$

$\omega_{ref} = 2\pi f_{main}$ (CB is closed: Synchronous operation)

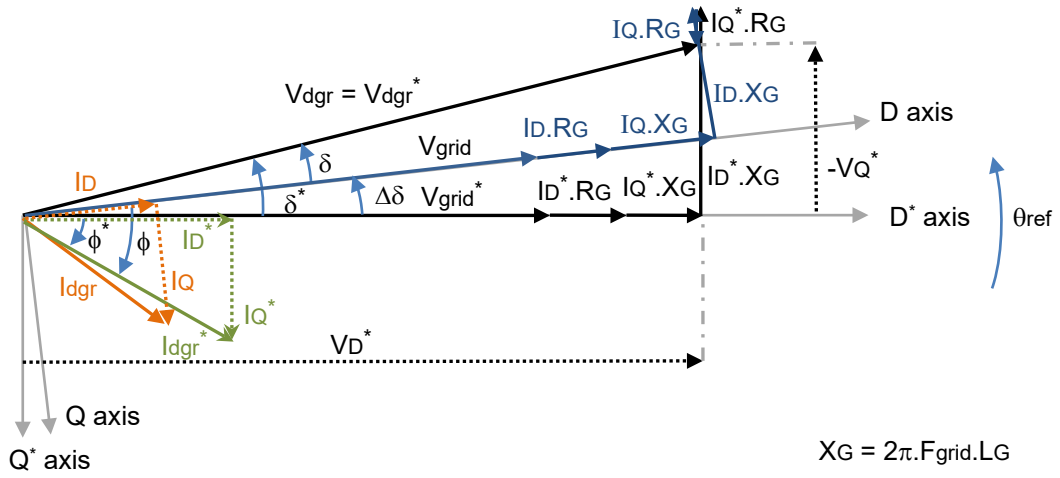




(DGR local phase shift for transformers, etc)

- 系統側とミニグリッド間の潮流測定
  - 目標有効電力／無効電力に応じて位相角⊿δを計算(Φglobal)
  - その値をMGCで全DGRに伝送
  - 電圧の大きさについてもMGCから伝送
  - DGR側でVgrid*とVdgr*を作成
- これにより潮流制御が可能になる
  - Vgrid*はMain Gridの電圧位相と一致するのでVdgrとの位相差がδ*になる
  - これにより両系統間を流れる有効無効電力潮流が決まる
  - 全体としてフィードバックループになる

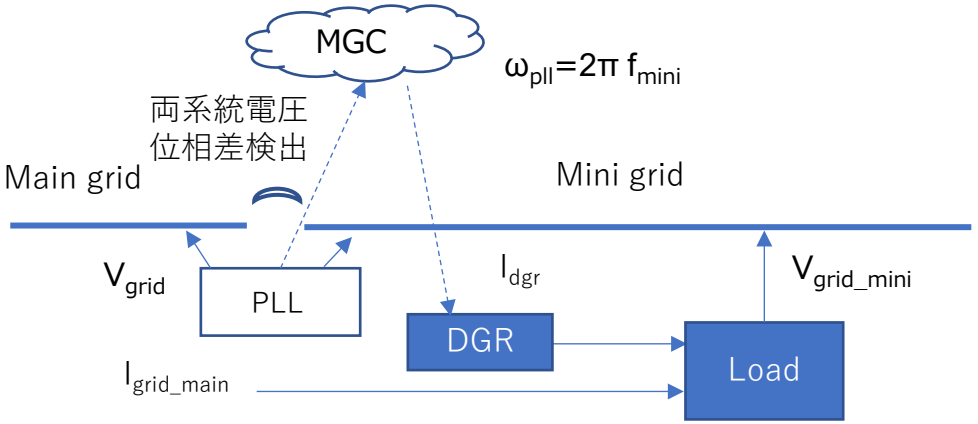
(2)系統分離時の位相同期

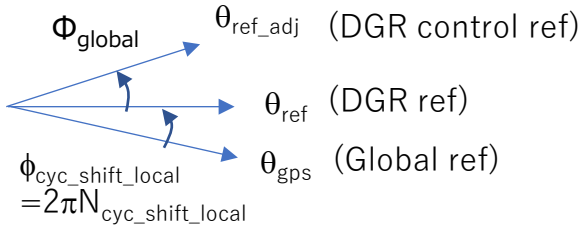


$X_G = 2\pi.F_{grid}.L_G$

- 系統側とミニグリッド間の電圧位相差測定
  - PLLで両系統の位相角⊿δを計算（Φglobal）
  - その値をMGCで全DGRに伝送
  - 電圧の大きさについてもMGCから伝送
  - DGR側でVgrid*を復元
  - フィードバックループになる
- これにより両系統の位相を合わせることがが可能になる
  - 遮断器の同期投入が可能となる

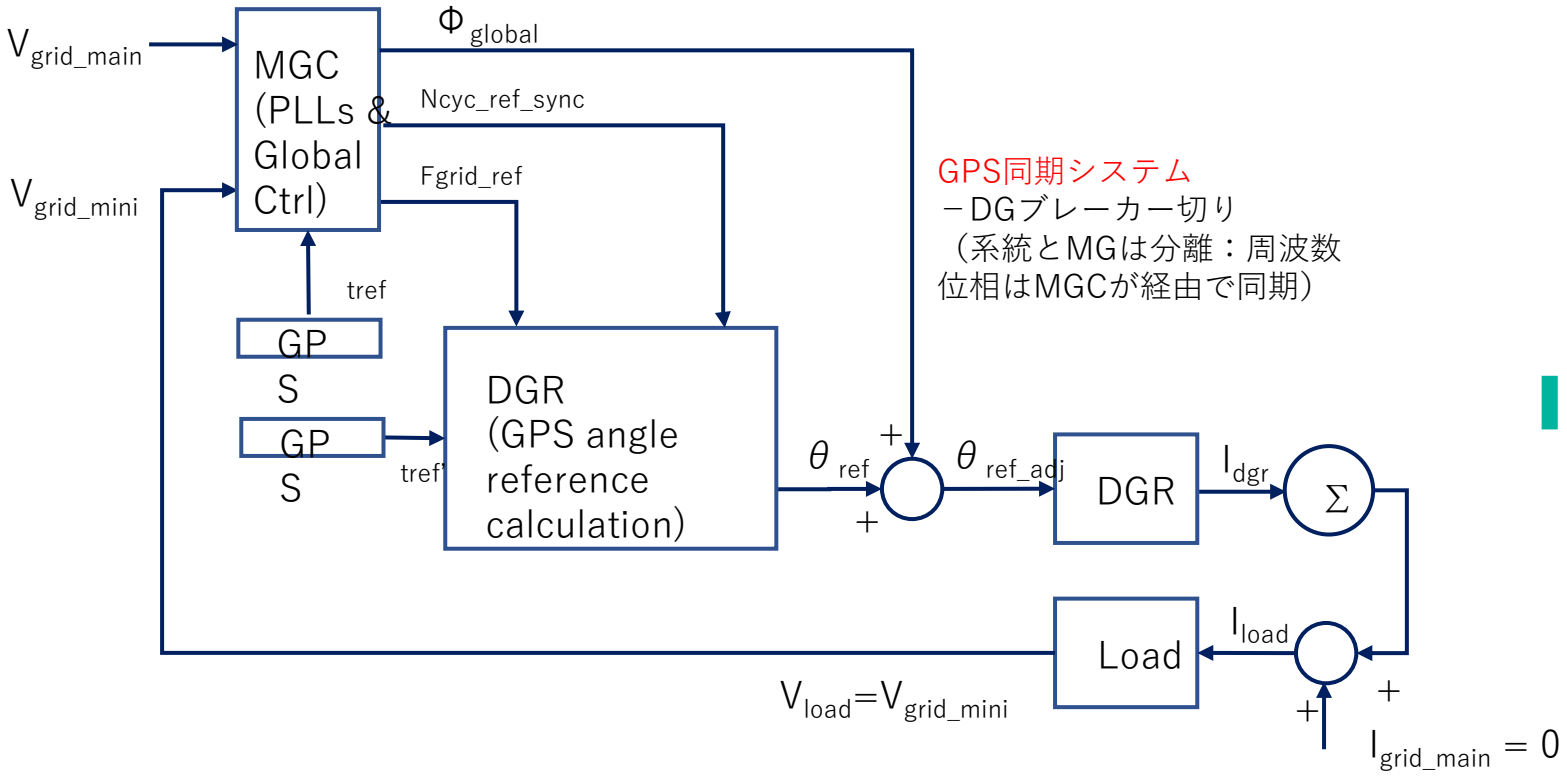
$\omega_{ref} = 2\pi f_{ref}$ (CB は開放: 非同期運転)





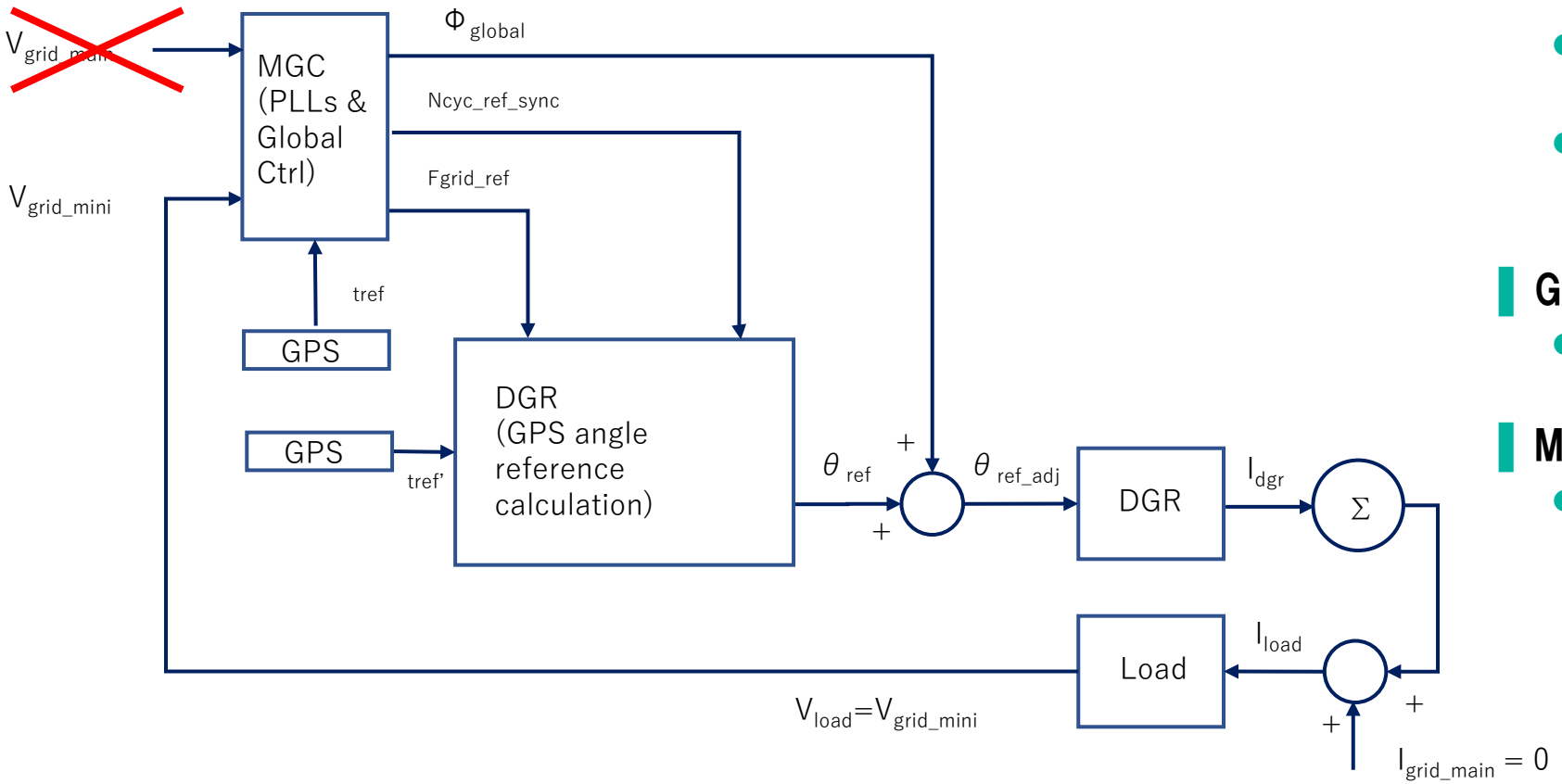
(DGR local phase shift for transformers, etc)

(3)系統遮断器の同期投入・無停電分離



- MGCには主系統とミニグリッド系統の両方の電圧が入力されそれぞれPLLで測定される
  - MGCで周波数と位相と電圧が伝送されている
  - GPS時刻同期で両系統は同期が取れている
  - Φglobalはオプションで調整機能を有する
  - これにより遮断器が開放されていても常に両系統の同期はどれている
- 両系統が接続されている状態から遮断器を開放してもミニグリッド系統は無停電で運転を継続する

(4)セルグリッドのブラックスタート



系統停電時

- MGCは内部に持つ電圧位相をリファレンスとして、ミニグリッドをブラックさせることができる
- GPS時刻信号で定めたタイミングでDGRは同時スタートできる
- ミニグリッド起動電流が大きい場合は一定時間持ちこたえることができるように設定できる

GPS信号異常時

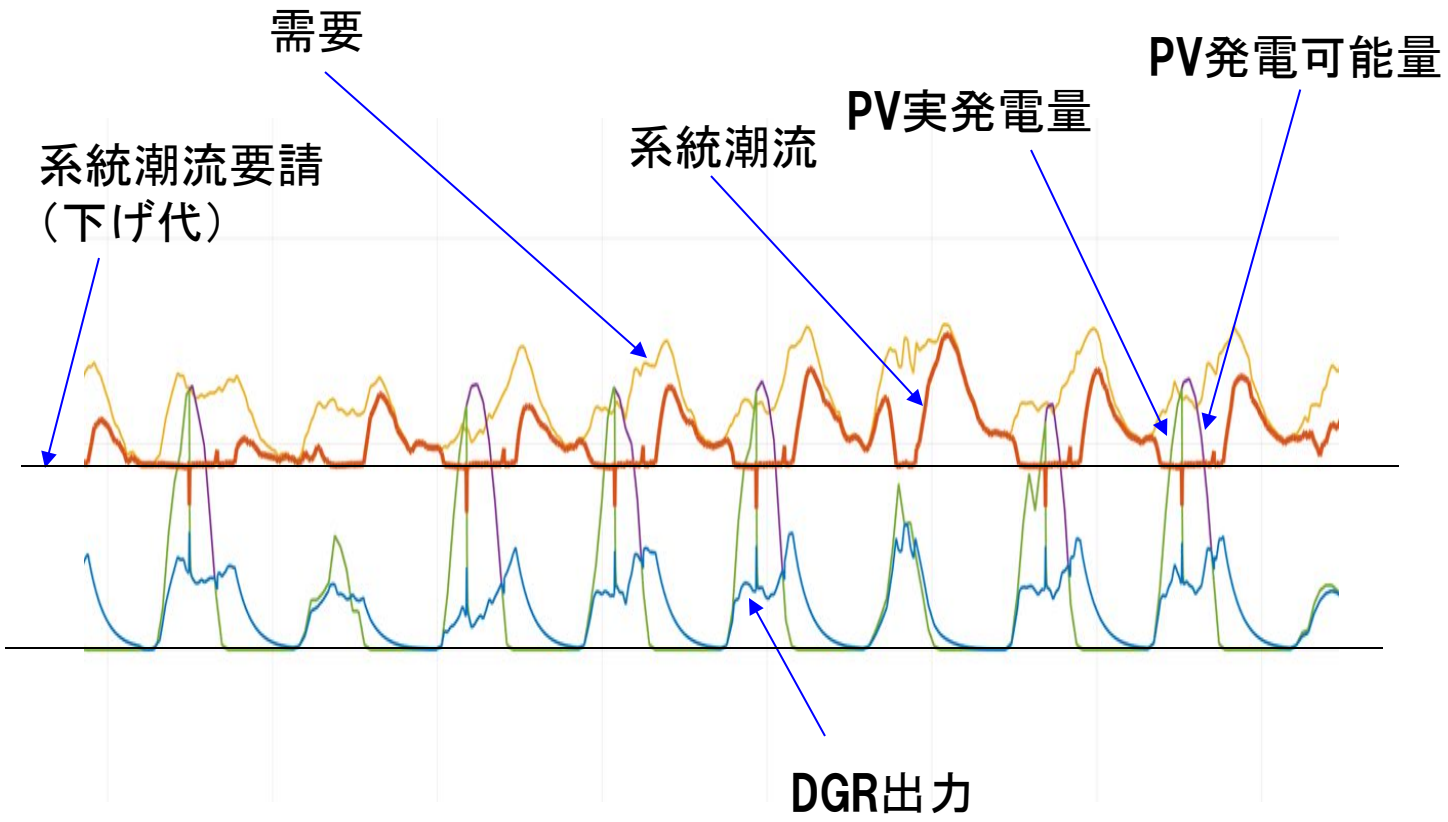
- 運転できていればPLL電圧モードに切り替えて運転継続できる

MGC異常時

- 運転できていればPLL電圧モードに切り替えて運転継続できる

5. 系統内DGR分散運転(ミニグリッドも含む)

(1)MGCによる調整力供給



- 左図はある離島におけるシミュレーションである
  - 島内発電所の下げ代不足により、最低出力を維持するよう求められている
  - 系統潮流を測定し、MGCでΦglobalを作成し、最低出力を維持するよう各DGRに伝搬している
  - それにより、最低出力を下回らないように運転が行われている
  - 需要変動部分はDGRが追従して出力している
  - 太陽光は発電可能量に対し、出力抑制が自動的にかかっている
- 発電所の潮流を更に細かく指定できる
  - 需要の変動分をすべてDGR群で吸収し、発電所を効率よく運転することも可能である
  - 予測制御の精度を上げ、蓄電池を活用すれば再エネ利用率を飛躍的に上げることができる
  - 発電所の下げ代を見直すことで、化石燃料使用量を大幅に削減することが可能となる。

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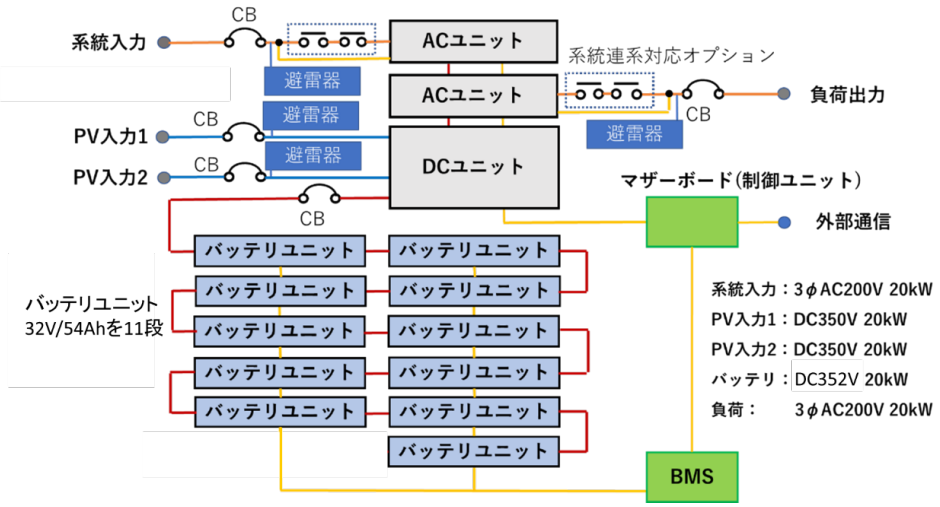
6. DGRによるビジネスモデル

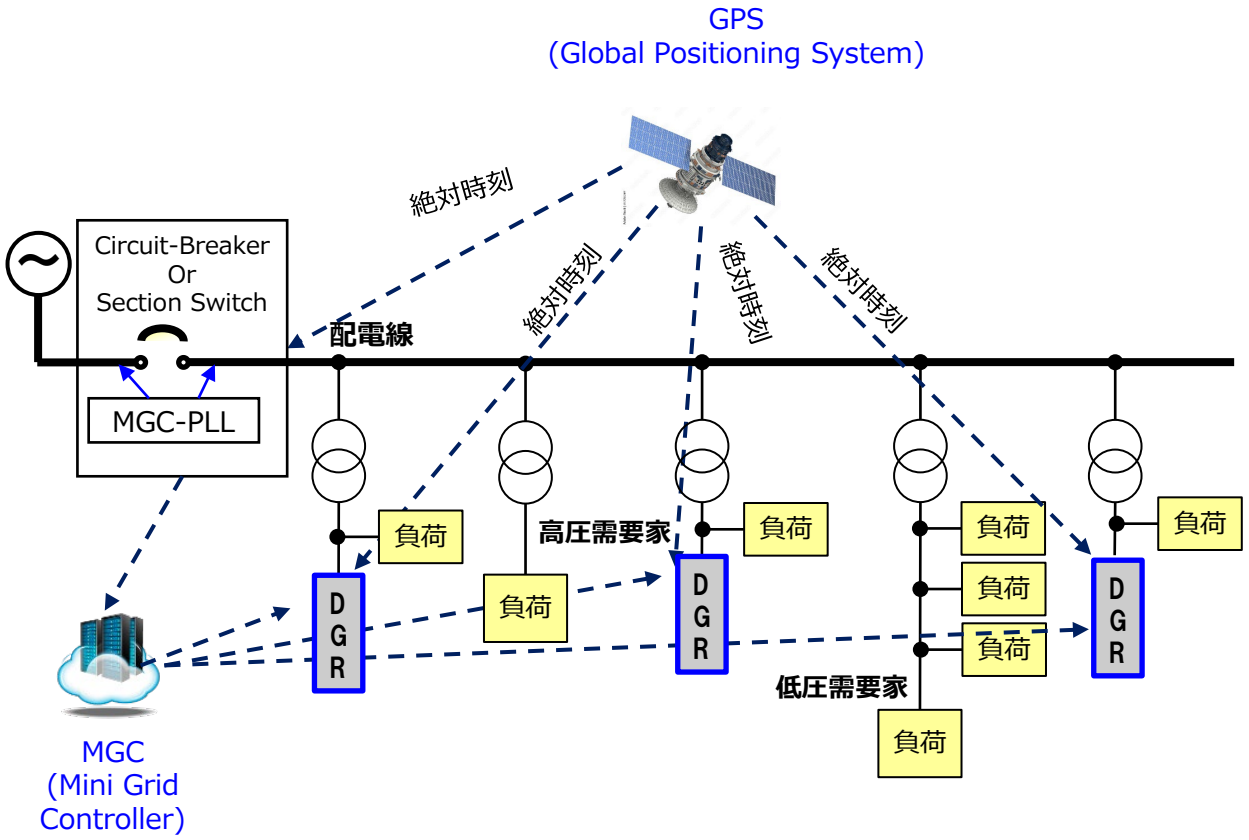
(7)DGRの価格低下シナリオ



- 細かいパーツに分けて大量生産
  - ACユニット、DCユニット、バッテリーユニット、制御ユニット、筐体に分けて、個別に大量生産可能とする
  - ユニットはPlug&Play方式、すなわちパワー部も制御部もコネクター接続、手動抜き差しで接続完了
  - 修理もユニット交換→保守コストの低下
- 使用部品は太陽光パワコンと同等仕様
  - パワコンが大量生産で安くなったと同じメカニズムで価格低下
  - 価格を支配する主要部品が電気自動車と共通
    ・インバータ
    ・バッテリー
  - 筐体の塗装なども自動車製造のラインが好適
- 製造メーカーは世界中に分散
  - データはCAD化してどこでも製造できるようになる
  - ハードウェアには制御機能部品がない
  - 性能は制御ユニットのソフトウェアで決まる

6. DGRによるビジネスモデル

(7)MGCと系統連系における認証プロセス

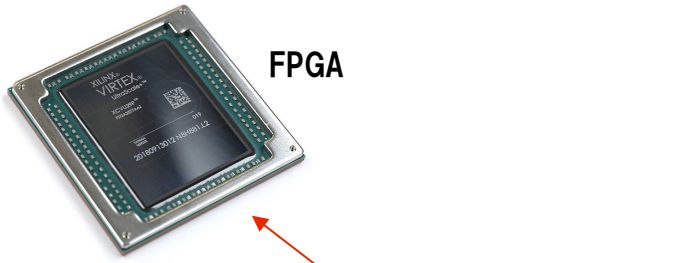


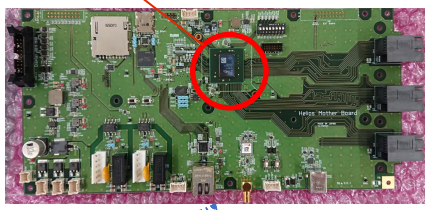
ソフト系によるMGCクラウド認証＋ハード系による電力系統連系認証

- DGRの使用にあたっては2つの認証プロセスがある
  - ソフト系のMGCクラウド認証
  - ハード系の電力系統連系認証
- モバイル回線を使用したソフト系のMGC接続認証
  - MGCが全DGRに情報を伝えるにはまず認証する必要がある
  - モバイル回線はセキュリティの観点から閉域網となる
  - 他者のなりすましは排除され、アタッキングも排除される
  - 系統位相情報などの伝搬サイクルを短縮できる閉域網
- 電力系統に接続するにあたっては系統連系認証が必要
  - 系統連系規定に準拠していること
  - 様々な保護機能と設定の確認を電力立会で実施
  - 運用に関する取り決めを契約
- デジタルグリッドコンソーシアムは上記認証を代行
  - DGR型式試験
  - DGR－ID発行
  - 認証マーク発行

7. オープンソースインバータ

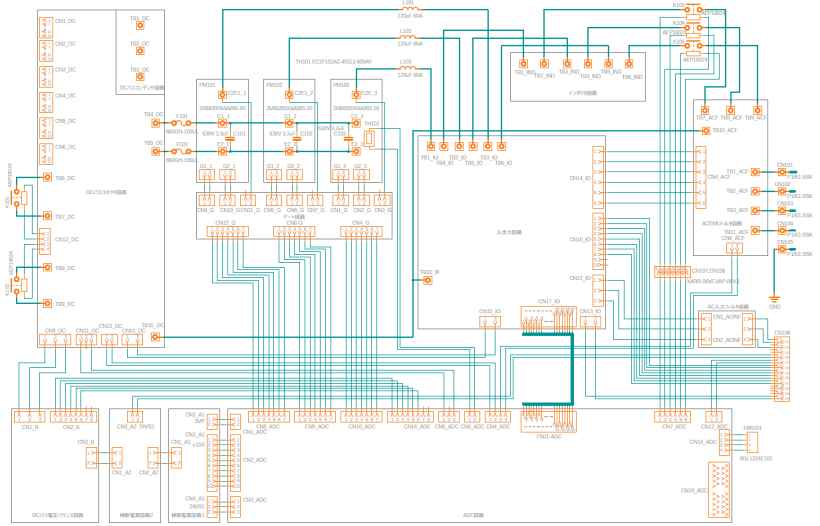
（1）DGRの制御チップ（FPGA+CPU）

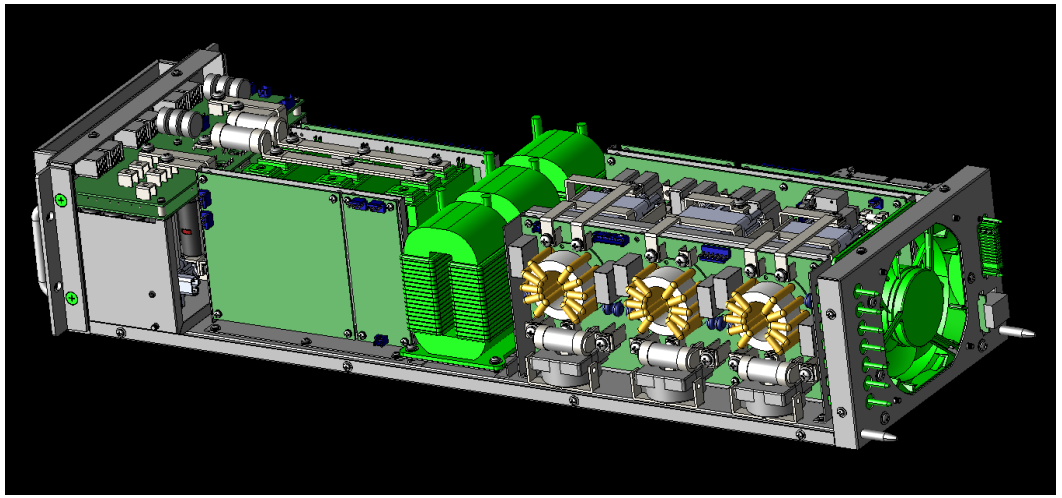




- **FPGA は、書き換え可能な論理回路集積IC**
  - PLD（プログラマブル ロジック デバイス）に分類される集積回路（IC）であり、製造後に変更できる適応性に優れたハードウェアで構築されている
  - 配列された各ハードウェア ブロックは個別に設定でき、必要に応じて接続できる
- **DGRの9つのハーフブリッジのヒステリシス用ゲート信号はこのFPGAから発信される**
  - すべての制御はこのチップに集約
  - モバイル回線を通じて書き換え可能
  - パワーユニット上には制御装置（マイコンなど）はない
- **割り込み機能がなく時間に忠実な制御が可能**
  - 太陽光の変動、バッテリーの状態、交流系統の変動、などすべての情報を集約して即座に応答
  - ヒステリシス制御と合わせて極めて高速
  - 50/60Hzの動きを40GHzで制御
- **このソースコードをオープンソース化予定**

(5)ハードウェア情報のオープンソース化





- ハードウェア情報のオープンソース化
  - 設計情報
  - CAD情報
  - 部品リスト
  - 製作図面
- 誰でもパッケージング化できるようにすべてをオープン化
  - 改造については各社のノウハウ化が可能
  - ライセンスフリー